Wet-Developable Organic Anti-Reflective Coatings For Implant Layer Applications

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Abstract

Bottom anti-reflective coatings (BARCs) have been widely used in conjunction with photoresists in the manufacture of semiconductors during the photolithography step of the process. The primary benefits of BARCs in photolithography are focus/exposure latitude improvement, enhanced critical dimension (CD) control, elimination of reflective notching, and protection of DUV resist from substrate poisoning. In the past, BARCs have mainly been used in critical layers such as gate and contact layers. As integrated circuit feature sizes continue to shrink, the application of a BARC in implant layers becomes more desirable because the tolerances of reflective notching and CD variations caused by wafer topography are getting smaller.

Wet-developable BARCs have been developed specifically for implant layer applications. The feasibility of using traditional dry-etch BARCs is very questionable because they introduce more process complexity and more defectivity and potentially cause unnecessary substrate damage. This paper will review the difficult challenges of producing implant lithography layers and discuss wet-developable BARC design criteria and requirements. This paper will also discuss the performance of wet-developable BARCs used in implant layer lithography and the technical challenges of the process.

Key words: optical lithography, anti-reflective coating, CD control, substrate reflections, implant, BARC, wet-developable

1.0 Introduction

The semiconductor industry's technology-driven transition to 65nm is expected to happen within a few years [1]. Optical lithography is still the desired approach due to its cost effectiveness. Many of the 248nm processes are mature, but they are continually being extended. Because of the significant progress in photoresists, anti-reflective coatings, optical proximity correction, off-axis illumination, and phase shift masks now allow an extension of 248nm deep ultraviolet (DUV) lithography to the 90nm node and even beyond. In the past few years, tremendous emphasis and resources have been applied to developing 193nm technology, including immersion lithography. The target is to bring the 193nm technology to the marketplace for the 65nm node or below in production [2-6]. At the same time, existing technology challenges and the ongoing 193nm lithography delays necessitated the extension of 248nm-based lithography far beyond what the industry had originally anticipated.

Feature sizes continue to shrink as demand increases for high-speed devices and more devices must be packed onto a die. New process steps emerge that require the use of enhanced anti-reflective coating strategies. Tight critical dimension (CD) control becomes more important than ever. This is also true in implant processes that traditionally count as "non critical layers"[7]

Ion implantation is an intermediate and key process during the fabrication of computer chips in the semiconductor industry. In the photolithography area, implant blocking layers have long been considered to be "non-critical" because their dimensions are at least two to three times larger than the sizes of isolation/gate/contact layers, which are usually regarded as "critical" layers. However, these designations have increasingly been challenged as transistor engineering requirements become more and more stringent.

Particularly, in contrast to isolation/gate/contact layers, an implant layer is often patterned on a wafer substrate with high topography and high reflectivity. The patterns of shallow trench isolation (STI) and poly gate are the main sources of high topography. Applying an organic or inorganic anti-reflective coating is often an inadequate process remedy because it not only introduces more process complexity but it also increases defectivity.

2.0 Implant Lithography Challenges

A typical 130nm logic process flow today may contain as many as 14 implant masking steps in which most of the layers need CD and overlay controls due to the budgetary limitation of line edge placement (LEP) error. Table 1 reviews the implant layer types typical for today's CMOS technology. In addition, several new challenges arise from a tighter LEP budget, such as requirements for more vertical resist profiles [7], more substrate stability of DUV resist, less implantation shadowing [7,8], and less reflective notching of resist patterns. In particular, reflective notching has been proven to play an important role in determining the device leakage failure rate. For example, the experimental results (Fig. 1) of a CMOS device with 0.18μm technology clearly indicate that the device leakage failure rate is strongly correlated to the resist line-width of the source/drain implant layer. However, the LEP error calculation indicates that there should be no evident leakage failure even at the 0.58μm line-width. Where does the leakage come from? Finally, we found that the leakage failure is due to the reflective notching. Because the severity of reflective notching is inversely proportional to the resist line-width, it is not surprising to get a leakage failure curve such as that displayed in Figure 1. In this paper, we will discuss how to reduce or eliminate the reflective notching for implant resist patterns by using a wet-developable bottom anti-reflective coating.

Table 1. Typical implant layers and requirements for today's CMOS technology.

Implant	CD as a multiple of gate CD	Implant Energy/Dose	Minimum Resist Thickness	Topography	Major Challenge
Well	4-5X	200-1000KeV 1e12-1e14	1.5-3.0μm	STI	Resist Profile
LDD	4-5X	15-100KeV 1e12-1e14	0.4-0.7μm	STI, gate	Topography
S/D	2-3X	10-50KeV 1e13-1e16	0.2-0.4μm	STI, gate	Topography
Vt adjust	4-5X	20-100KeV 1e11-1e14	0.5-0.7μm	STI	Topography
Contact	4-5X	20-100KeV 1e14-1e17	0.4-0.7μm	contact	Topography PR poisoning

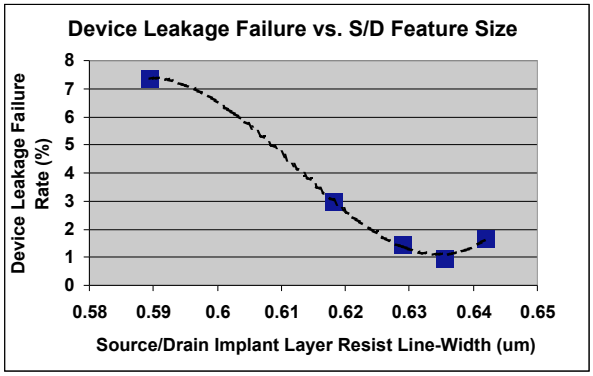


Figure 1. Device leakage failure vs. S/D feature size.

3.0 Wet-Developable BARCs

While dry-etch organic BARCs are used extensively for critical lithography layers requiring plasma pattern transfer, they typically cannot be used for implant layers for the following reasons:

1) The etch process to clear the BARC is complex. Controlling the etch end point is very difficult, which makes the implant and diffusion process also difficult to control.
2) Adjusting implant energies to penetrate appropriately through the BARC layer is difficult. The BARC thickness may vary in relation to local topography.
3) Ions used for the dry-etch step are highly energetic and may participate in the implant and diffusion process to decrease the efficiency of silicon performance.

Like any other BARCs currently on the market, a wet-developable BARC is an organic liquid coating material used in conjunction with a photoresist during the photolithography step of the process to manufacture semiconductors. The difference between a wet DUV BARC and a dry-etch BARC in the lithographic process is that a wet DUV BARC is soluble in developer so it can be removed during the resist development step. Figure 2 describes the differences between dry- and wet-patterning BARCs.

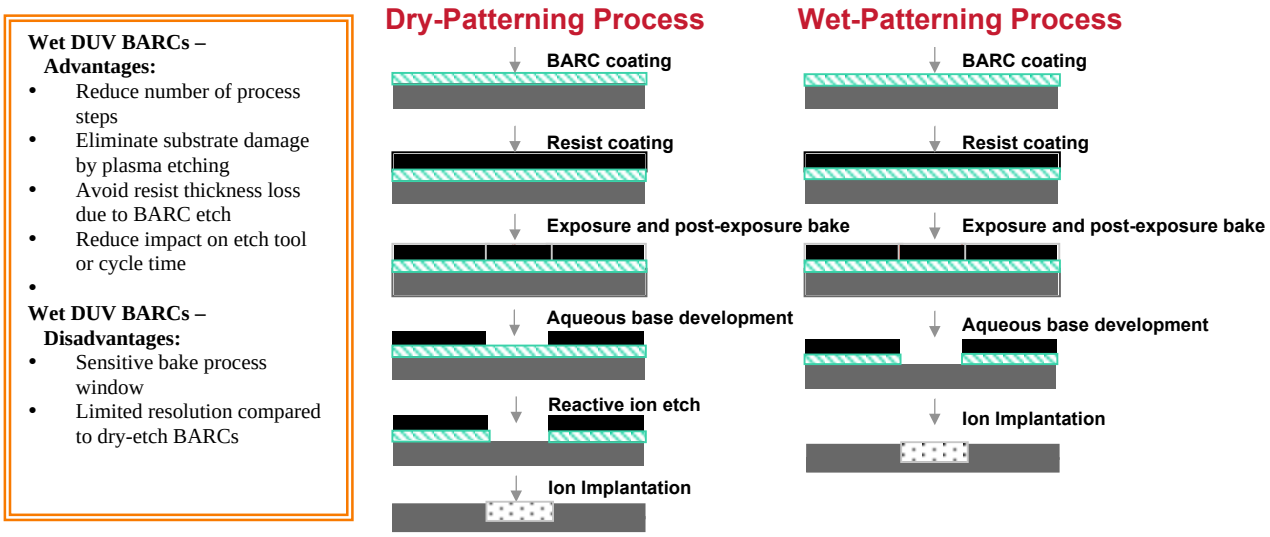


Figure 2. The comparison of wet-partterning and dry-patterning processes.

Additionally, the high standards of the semiconductor industry require the following from a wet-developable BARC:

1) Equal to or less than 0.18μ resolution
2) Side walls as straight as those produced by a dry-etch ARC
3) Spin-bowl compatibility
4) Safe solvent system
5) Room temperature stability
6) Low wafer defects
7) Broad bake process window
8) Equal to or less than 60 seconds for development time (with resist)
9) 200 and 300mm process conditions
10) Ability to be removed with industry standard strippers
11) Broad resist compatibility

Wet-developable BARCs were first introduced by Brewer Science in the early 1980s [10-12]. Traditionally, these BARCs have been based on a polyamic acid platform where the solubility of the BARC in aqueous developer is controlled by the BARC bake process. A representation of the imidization process is shown in Figure 3.

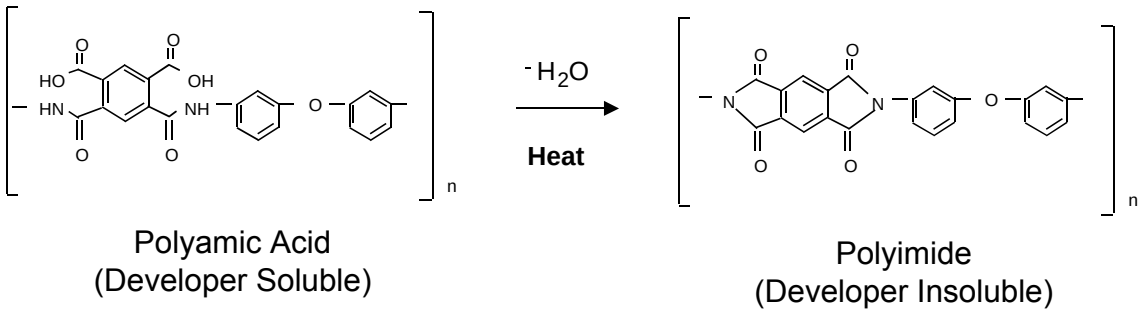


Figure 3. Example of wet-develop chemistry based on polyamic acid.

The solubility of the BARC in aqueous developer is controlled by the BARC cure temperature. During this stage the developer-soluble polyamic acid is converted into a polyimide, which is not soluble in base developer. For this type of BARC, a number of factors contribute to the dissolution of the material in developer, including transport of the developer to the surface; adsorption of the developer to the surface; the development reaction; desorption of the reacted product from the surface; and finally transport of the product away from the surface [13].

The dissolution rate of the BARC then is dependent on the degree of BARC cure. A bake latitude is defined by the upper and lower temperatures that induce line collapse and scumming between lines or in open spaces. (Fig. 4) It then follows that the best resolution is found in this bake "window" where the BARC undercutting and footing are controlled.

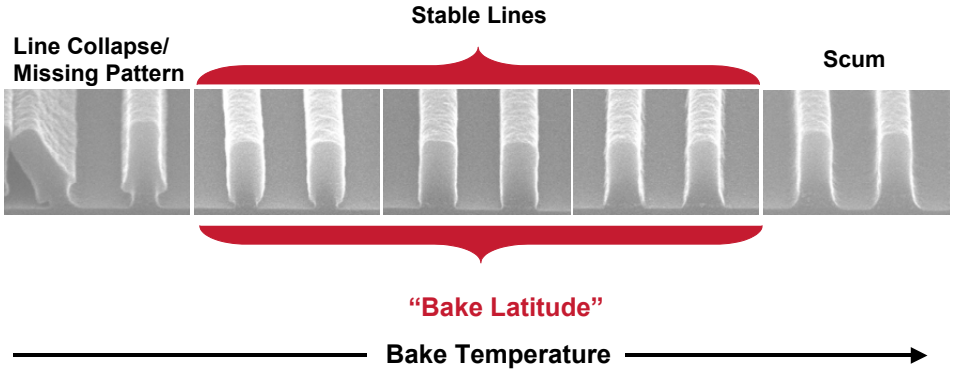


Figure 4. Illustration of bake latitude for a wet-developable BARC.

4.0 Implant Application with Wet-Developable BARC

4.1 Reflective Hole Improvement

In the 130nm technology node, how to define a notching-free S/D implant layer is a challenge for the process engineer. The difficulty arises mainly due to the reflective light from the sidewall of STI. Usually, after generating STI and then filling SiO_2 into the trench, chemical mechanical polishing (CMP) will be applied to the wafer to remove the main topography. However, because SiO_2 is a transparent material, the reflective light still plays an important role in damaging resist patterns.

In order to understand the detailed mechanism that caused the reflective notching, we did a Solid-C simulation for a special pattern of S/D implant layer. The pattern consists a rectangular STI opening filled by SiO_2 and then covered by a rectangular resist. The simulation (Fig. 5) predicts that the reflective light from the STI sidewall is mainly focused at the four corners of a rectangular resist pattern, and therefore four reflective holes on the resist pattern will be observed after the exposure and develop steps. Our experiments proved the predictions from the Solid-C simulation. In Figure 6(a), due to the reflective light

from the STI, four resist holes accompanied with rough edge near the corners were observed. Fortunately, after applying the wet-developable BARC (IMBARC™), all resist damage to the nearby four corners were removed (Fig. 6(b)).

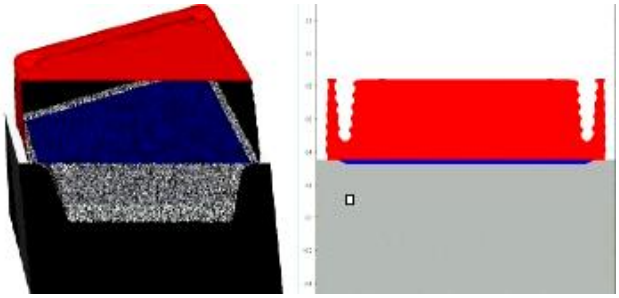
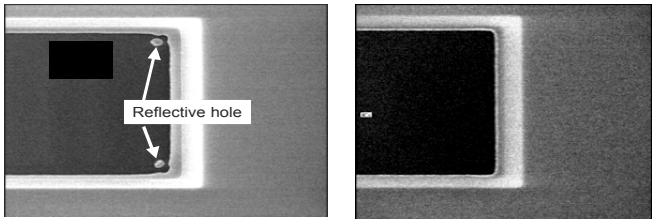


Figure 5. Solid-C simulation predicts that since the reflective light from the STI sidewall is focused at four corners of a rectangular resist pattern, four resist holes will be observed after exposure and develop steps.



a) Without BARC b) With IMBARC™

Figure 6. Solid-C prediction was proven by our experiments. The top-down SEM photo (a) indicates that not only four resist holes but also the rough resist edge introduced by the reflective light from STI were observed. Fortunately, applying the developable BARC (IMBARC™) provided a solution (b).

4.2 Process Window Improvement

It is well known that reflective notching can damage the process window (PW). We used a standard S/D implant layer as an example [7]. This layer was processed by using 0.65μm Shipley UV5 resist with illumination conditions NA= 0.57 and σ=0.45 (Fig. 7). If the resist features without the notching were measured, the PW showed a rectangular shape with 0.6μm DOF and 40.45% exposure latitude (EL). However, the effective PW was severely damaged by reflective notching (Fig. 8(a)). The finally useful PW was limited within the area indicated by a dotted line in Figure 7. Although the PW can be improved by using more incoherent illumination [9], this compromise can sometimes fail to provide a good pattern definition, particularly in the cases where the resist hole and line coexist in layout.

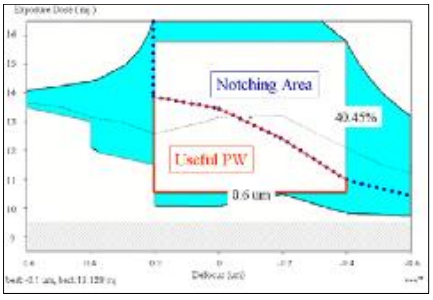
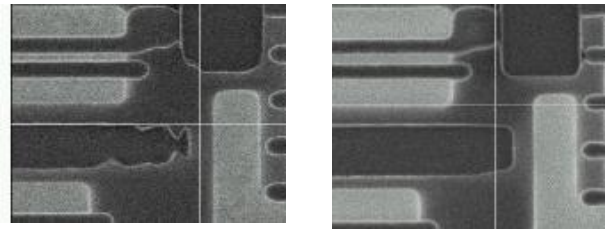


Figure 7. More than 50% of the process window is lost at a S/D implant layer in 0.15μm technology node. The illumination conditions used in the process are NA=0.57 and σ=0.45



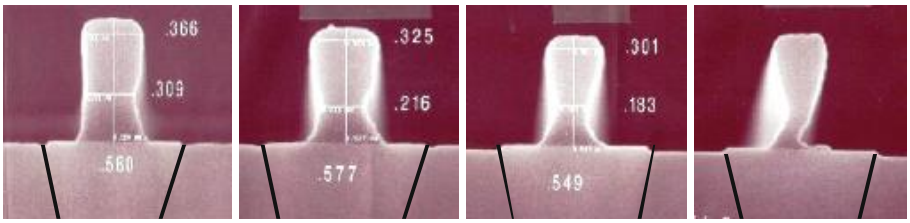
(a) (b)

Figure 8. The resist pattern of an S/D implant layer in 0.15μm technology node was used in generating the process window in Figure 7. Due to the topography from STI and poly gate, the severe notching can be observed in (a). After using IMBARC™, the reflective notching was removed totally (b).

Fortunately, using IMBARC™ provided the possibility to remove the reflective notching totally without compromising the illumination conditions (Fig. 8(b)).

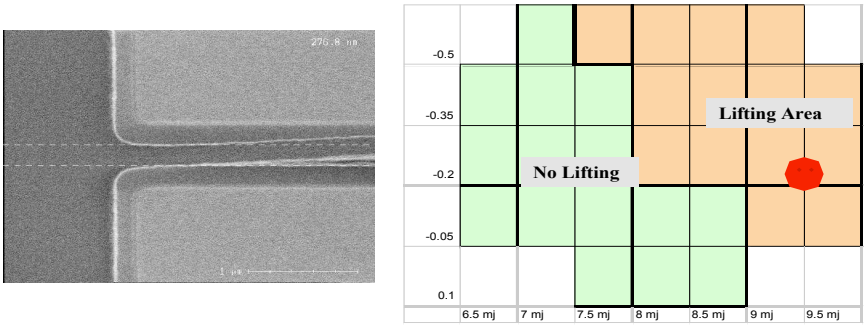
4.3 Resist Lifting Improvement

In an S/D implant layer, the reflective light from STI profile may also introduce resist lifting. The severity of resist lifting is dependent on the exposure dose (Fig. 9). To avoid resist lifting, a lower exposure dose may be needed. However, getting nominal CD size then becomes impossible without resist lifting (Fig. 10).



(a) (b) (c) (d)

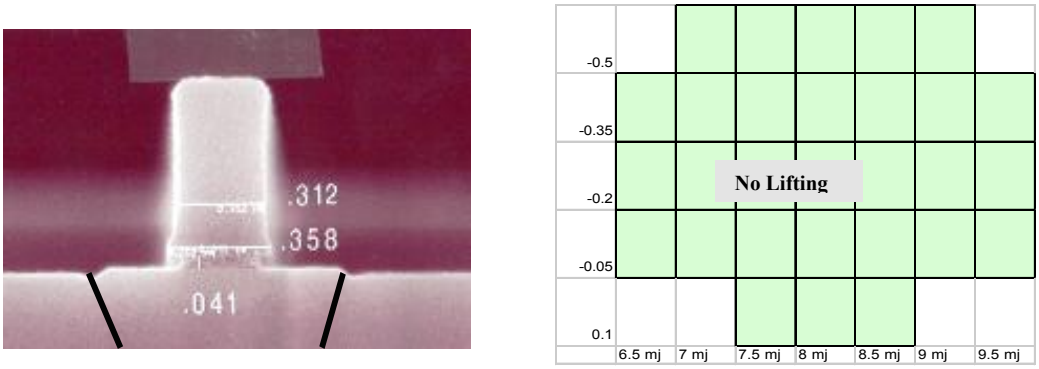
Figure 9. A resist line sitting on the trench oxide after CMP was lifted by gradually increasing the exposure dose from (a) to (c) due to the reflective light from STI. The tilted lines in substrate are the profile of STI.



(a) (b)

Figure 10. A 0.3μm resist line was lifted due to the reflective light from the slope of STI (a). The focus exposure metrics (FEM) results shown in (b) indicate that it is impossible to obtain a nominal CD size without resist lifting.

The IMBARC™ application eliminated the resist lifting totally (Fig. 11). The corresponding PW without resist lifting was increased significantly. The process can be easily defined either at the nominal CD or at an even lower CD. However, the IMBARC™ process needs to be optimized further because the SEM cross-section showed some slight undercutting (Fig. 11(a)).



(a) (b)

Figure 11. The IMBARC™ application removed the resist lifting totally, as shown in (a). The FEM results all showed that no resist lifting exists in a wide dose and focus range, as shown in (b). However, the IMBARC™ process still needs to be optimized further because the cross-section in (a) indicates that some undercutting is still there.

5. Wet-Developable BARC Challenges

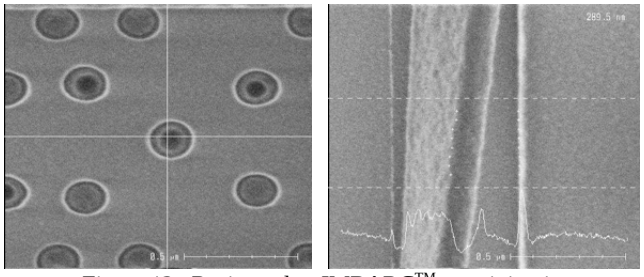
5.1 BARC Process Optimization

The implementation of a wet-developable BARC such as IMBARC™ requires selection of appropriate film thickness as well as the optimization of both bake and develop processes. The selection of BARC thickness not only affects the reflectivity control for a given substrate and film stack but can shift the optimum bake window.

The dissolution rate and hence the degree of undercut or foot of the wet-developable BARC is most easily modified through the bake process. In the case of IMBARC™ the bake temperature has the greatest impact on develop rate with bake time a secondary parameter. (Figure 4.) Once near the optimum bake temperature the bake time can be used to fine tune the desired profile.

5.2 Residue Remaining on Poly/Oxide/Contact Implant Structures

The removal of resist and BARC in between fine features or over deep topography is a distinct challenge for this generation of wet-developable BARCS. The clearing of BARC and resists out of a contact hole or between poly lines or clearing resist patterned over trench topography must be evaluated for critical areas. Smaller feature sizes limit develop transport to localized regions on the substrate. Figure 12 shows residue remaining in implant contact holes. Figure 13 is another example of residue remaining in 0.0µm contacts and residue left behind between poly lines <100nm space. Depending on the application, developer and rinse processes may be used to improve removal of the residue. Reduced bake temperature (enhancing develop rate) could also be used but there is a trade-off with potential degradation of the resist/BARC lithography profile.



IMBARC™ 20-7
RPM: 2.5K
HP: 130ºC/30 s
175ºC/60 s
Single puddle/rinse
0.65μm ESCAP1

Figure 12. Resist and or IMBARC™ remaining in contact implant.

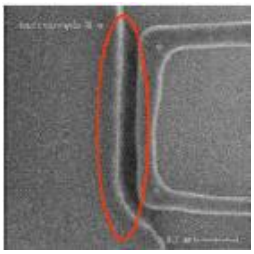


Figure 13. Residue between resist and poly line (~80nm).

6.0 Conclusions

Using a wet-developable BARC in an implant layer application is a new approach for achieving tight CD control without damaging the substrate. It is clearly demonstrated in this paper that IMBARC™ enables the elimination of resist notching/holes and improves the process window for exposure latitude and depth of focus which without the BARC is limited by reflective notching. Additionally, the use of IMBARC™ completely eliminated resist lifting and significantly improved the process window.

The main challenge for applying our current wet-developable BARC (IMBARC™) in an implant layer is the residue that remains after resist/BARC development, which is caused by incomplete development. This challenge is particularly apparent when the application has a relatively high topography (>150nm) and the space is small (<100nm). While a somewhat effective remedy is achieved by applying process variations such as double rinse, double puddle development, etc., we are working very hard to solve this problem by adjusting the BARC development rate through chemical modification in the BARC systems.

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