New developer-soluble gap-fill material with fast plasma etch rate

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ABSTRACT

For the via-first dual damascene process, a planarizing anti-reflective material or gap-fill material is typically used to ensure a lithography process produces the best profiles and critical dimension (CD) control. These requirements pose many challenges to material scientists, and the most difficult task is likely to be designing spin-on materials that provide zero bias between dense and isolated pattern areas. We have developed a unique solution, in the form of wet gap-fill (WGF) materials, to further reduce both iso/dense bias and the overall process time.

In order to reduce iso/dense bias, dry gap-fill materials are used in combination with a plasma dry etch-back process. However, the bias reduction is less than satisfactory because the initial coating bias will transfer to the final surface through the etch process. As their name implies, our WGF materials fill surface topography and utilize a standard photoresist developer to etch back to the substrate surface. These WGF materials, by careful design, aim to minimize bias caused by the difference between the faster bulk material dissolution rate and the slower rate in small vias. After wet etch back, the isolated and dense via-patterned areas both are fully filled, and the bias is much smaller than the bias of the initial coating. In contrast to the dry etch-back process, wet etch back eliminates the need to transfer wafers between the etch and photo bays, which is definitely financially favorable. In addition, future low-k materials will most likely be porous, which raises the concerns about etch damage. Wet-etch gap-fill materials will provide an ideal solution to this problem.

Keywords: wet gap-fill (WGF), dual damascene (DD), via, iso/dense bias, process window, planarization, etch, low-k

1. INTRODUCTION

The driving force behind growth in the integrated circuit (IC) industry has been the continuous shrinking of the transistor. By making the transistor faster, smaller, cheaper, and more efficient, electronic devices become more portable and accessible. As the feature sizes shrink and the density of transistors on chips further increases, the electrical resistance and parasitic capacitance with back-end-of-line aluminum interconnections have grown into major factors that limit the circuit speed of high-performance ICs [1]. To overcome these problems, the copper dual damascene (DD) process for metal interconnection and low-k materials for interlayer dielectrics has been integrated into IC device fabrication.

Among different DD processes, the one most commonly used is the so-called via-first DD process [2,3]. In this process, deep vias are formed first, then trenches are patterned on top of the vias. A planarizing gap-fill material is needed to ensure the trench-patterning process produces the best profiles and critical dimension (CD) control [4,5]. This gap-fill material not only reduces the surface topography but also prevents over-etching the underlying metal or transistor structures at the base of the vias while the trench is being etched.

One important property of a gap-fill material is the ability to fill the gaps properly without forming any voids. Void formation causes non-uniform etching and leads to some vias being insufficiently protected by the via-fill material during the trench etching. The thickness of the gap-fill material over dense vias is different from that over isolated via areas, which is called iso/dense bias. The degree of bias depends on many factors such as via size and via distribution. A good gap-fill material should be able to reduce the bias, which in turn decreases the variation in resists thickness and ensures good CD control. During the trench etch, a serious problem is the formation of "fences" or "crowns," which are caused by the deposition of dielectric etch by-products that form residues surrounding via openings. If the etch rate of a gap-fill material can be tuned to match that of the dielectric, it will greatly reduce the fencing effect and problems in after-etch cleaning. Porous dielectric materials will likely become a standard as lower k-values are required. These

porous layers will have faster etch rates than currently available materials, so there will also be a demand for gap-fill materials that have fast etch rates.

Currently one of the popular gap-fill strategies is the so-called dry etch-back process. Vias are first filled using a thick spin-on film and then a plasma etch is used to remove material to clear the wafer surface and leave only filled vias. However, the bias reduction is less than satisfactory because the initial coating bias will transfer to the final surface through the etch process.

As an alternative, we propose a wet etch-back process using a standard photoresist developer to remove the gap-fill material back to the substrate surface. By carefully designing the dissolution property of gap-fill materials, it is possible to reduce the initial bias from the coating and provide a better planarized surface for the ensuing lithographic process. It is also possible by design to enable the gap-fill material to be cured during the process or remain soluble to developer even after trench etch. The latter scenario provides an ideal solution to the problem related to etch damage on porous low-k materials. However, it would be an enormous task for one material to meet all the requirements discussed thus far, and realistically, some compromises have to be made. However, no matter what properties the wet gap-fill material has, all wet etch-back processes share a common advantage: they eliminate the need to transfer wafers between the etch and photo bays (Figure 1), which is economically favorable.

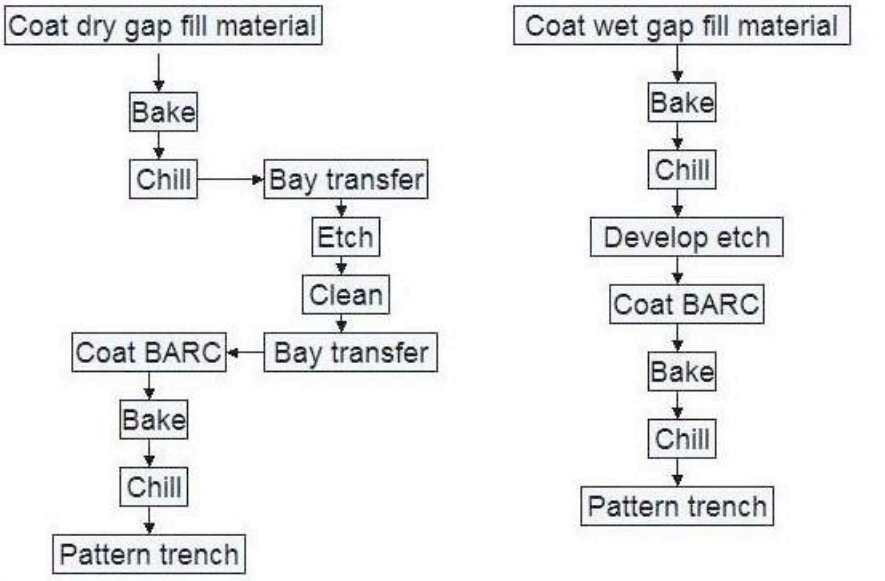

Fig. 1. Process comparison of dry etch-back and wet etch-back processes.

2. EXPERIMENTAL

2.1 Synthesis and formulation

Reaction temperature, time, and catalyst were adjusted to obtain the desired polymer properties. The formulations were prepared by blending appropriate amounts and types of polymers, additives, and solvents. The final solutions were filtered through a 0.1-μm filter.

2.2 Characterization

Polymer molecular weight and thermal, rheological, and optical properties were characterized. The dissolution rates of formulations were measured on a resist development analyzer (model 790, Litho Tech Japan). The formulations were

spin coated onto wafers at spin speeds ranging from 1000 rpm to 3000 rpm for 60 seconds and then baked using a Cee 100CB combination spinner/hotplate. The developer used was standard 0.26N TMAH.

2.3 Gap-fill tests

Topography wafers were used for via-fill testing. The formulations were spin coated onto silicon wafers and then baked. A set of wafers was coated and baked, developed for different lengths of time, and then rinsed. The cross-sections of all coated wafers were examined using a scanning electronic microscope (SEM).

3. RESULTS AND DISCUSSION

3.1 Stripping in solvents

After wet-etching back to the top of the via, usually a layer of anti-reflective coating would be applied. If the gap-fill material is soluble in the solvent used to make the anti-reflective coating formulation, intermixing will occur. Too much intermixing will most likely alter the optical parameters of the anti-reflective coating, change the fill character of the fill material, and result in the formation of voids. Therefore a stripping test was performed to ensure that the gap-fill materials, after curing, do not dissolve in solvents commonly used in anti-reflective coatings and resist formulations. Samples EXP05013 and EXP06010 both have good stripping resistance, as the thickness change before and after stripping is only a few nanometers. The stripping property is closely related to the degree of crosslinking, which is in turn linked to process conditions. Figure 2 demonstrates the relationship between bake temperature and the film loss at the strip test.

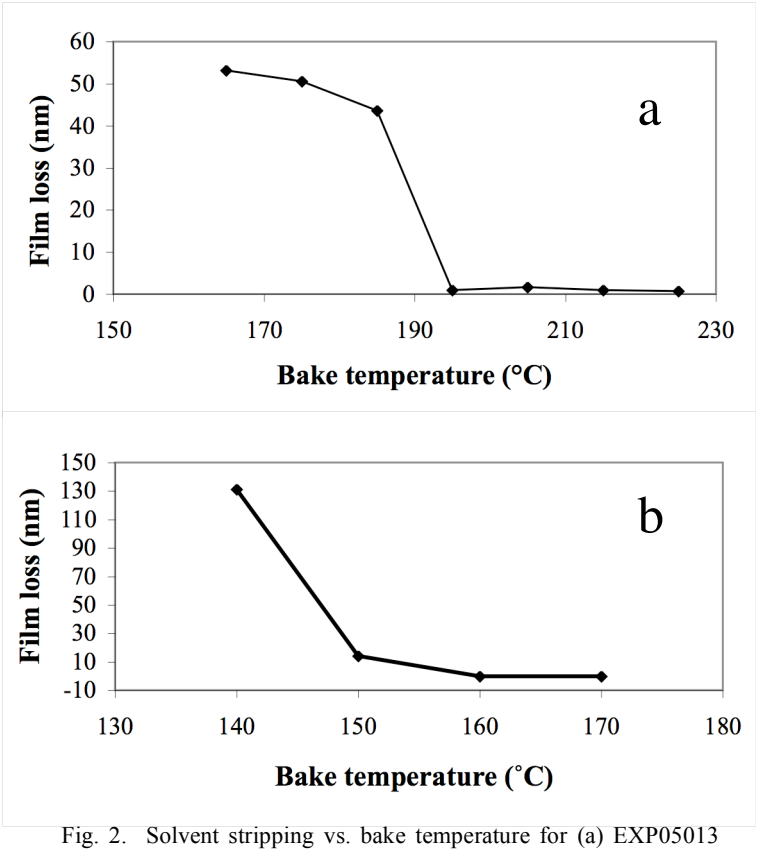

Fig. 2. Solvent stripping vs. bake temperature for (a) EXP05013 (ethyl lactate) and (b) EXP06010 (70/30 PGME/PGMEA).

The dissolution rates of gap-fill materials in standard resist developers were measured on a resist development analyzer. The operation principle of the analyzer is based on interference of 470-nm light. If a material's refractive index and

dissolution rate are constant during the dissolution process, and the material is also transparent at the wavelength of the exposure light, then a sinusoidal interference pattern caused solely by the steady depletion of the film thickness will appear. It is well known that the dissolution process consists of a few stages such as solvent diffusion, polymer swelling, and dissolving. Each stage is affected by a host of factors, for example, molecular weight and structure, acidity, the ratio of base-soluble groups, ion strength, polarity, etc. These factors not only determine the dissolution rate but also affect the physical behavior of the solute (for instance, swelling or cracking), which is closely related to the poor performance of the gap-fill material and which is usually manifested as peeling and void formation. Figure 3 shows the dissolution curves of our samples recorded on the resist development analyzer. The periodic interference pattern indicates steady dissolution rate and an indiscernible amount of swelling.

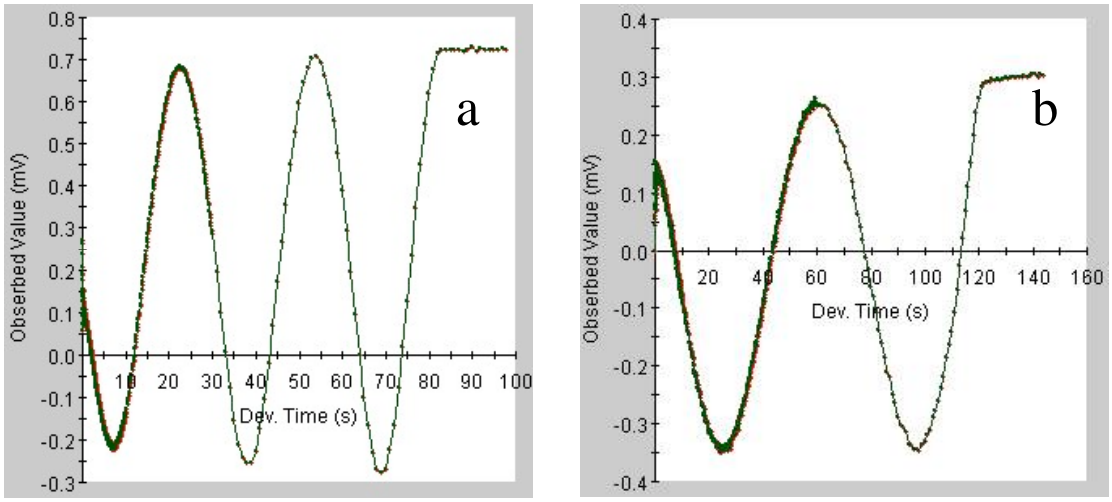

Fig. 3. Dissolution curves of samples (a) EXP05013 and (b) EXP06010.

3.2 Dissolution Rate

As mentioned above, the dissolution rate is affected by polymer molecular weight. It is conceivable that, for a given system, molecules with shorter chains are more mobile and easier to move into the solution. As molecular weight increases, so does the entanglement between molecules, which results in slower dissolution rates. Figure 4 shows the relationship between dissolution rate and molecular weight.

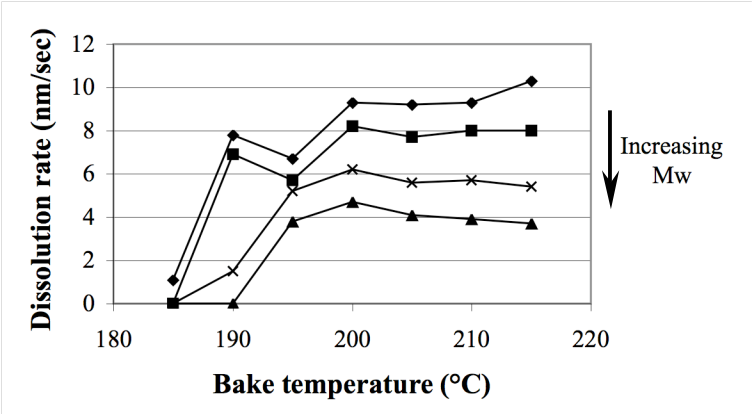

Fig. 4. Dissolution rate vs. bake temperature for EXP05013.

The dissolution rate is one of the key factors used to evaluate a WGF material. If the dissolution rate is too high, that is, the process time is too short, large film thickness variations may occur due to the difficulty of time control. On the other hand, a very slow dissolution rate reduces throughput. Usually rates ranging from 2 nm/sec to 10 nm/sec provide a balance of wet etch-back accuracy and process time. The dissolution rate can be adjusted many ways. One common method is formulation modification. For example, varying the amount of catalyst in EXP05013 alters the base solubility of the polymer, which in turn changes the dissolution rate. This relationship is illustrated in Figure 5. This property allows for customizing the development rate without changing the base chemistry, a very useful property that allows these materials to be used in potentially many different applications.

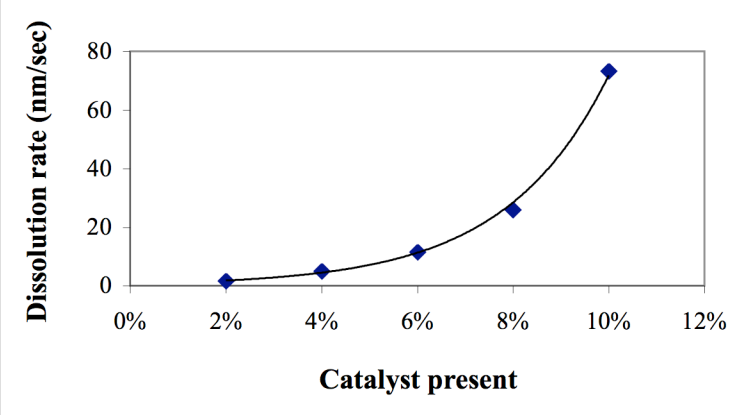

Fig. 5. Dissolution rate vs. catalyst loading for EXP05013.

The dissolution rate is undoubtedly influenced by process as well. In the IC industry, quality control demands a wide process window to minimize the uncertainty caused by tool limitations. Sample EXP05013 has a very large process window; Figure 4 indicates that its dissolution rate is almost constant when the bake temperature is higher than 195°C. Sample EXP06010 has a dissolution mechanism different from that of sample EXP05013, and its dissolution rate (Figure 6) changes very slowly with bake temperatures below 150°C [<0.1 nm/(sec × °C)]. This also provides a large process window, especially for modern tracks that have temperature control as accurate as ±0.25˚C in the low hot plate temperature range (<180˚C).

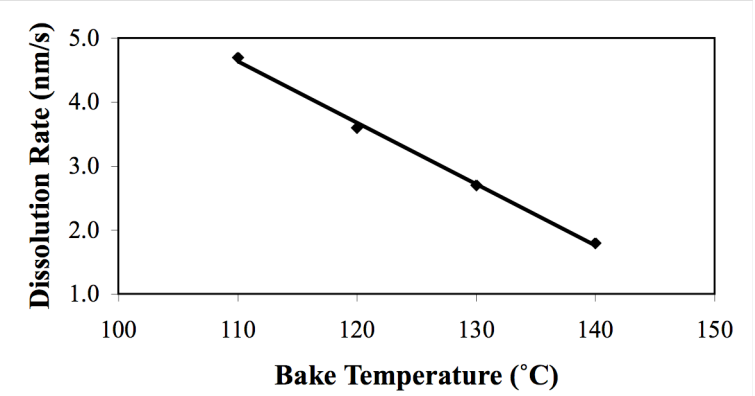

Fig. 6. Dissolution rate vs. bake temperature for EXP06010.

3.3 Via fill and iso/dense bias

A via-fill material faces two challenges: one is to be void-free and the other is to effectively reduce iso/dense bias. Voids are usually caused by trapped gas bubbles that may be caused by vaporizing solvent and/or gases released from the chemical reaction during baking. By adjusting the formulation and process conditions to balance both the gas release rate and the solidification rate of the gap-fill material, voids can be eliminated. Figures 7 and 8 show SEM images of the gap-fill cross-sections for both EXP05013 and EXP06010. The diameter and depth of the vias shown in Figure 7 are similar to the size found in a 65-nm node device. No voids were found in these small structures, and we expect that these materials will be applicable to 45-nm and smaller nodes.

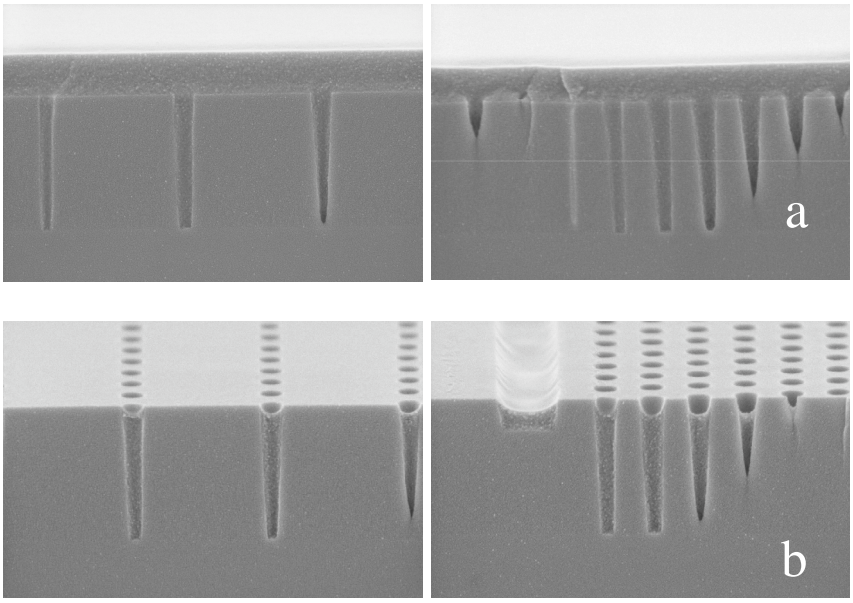

Fig. 7. Wet etch-back performance of EXP06010. Via wafer coated and (a) baked at 130°C for 60 seconds, and (b) baked at 205°C for 60 seconds after a 70-second wet etch-back (140-nm via diameter, 800-nm depth, 1:1 dense area duty ratio, and 1:5 iso area duty ratio).

Iso/dense bias reduction is more difficult to achieve. During the spin-coating process, evaporation of solvent quickly reduces the material's mobility before large topography can be planarized across the wafer. In a dense via area, a much larger via volume must be filled than that in an iso via area, therefore the film thickness on top of the dense area is markedly thinner than that on top of the iso area. The iso/dense bias can be improved by modifying process conditions, molecular weight, material viscosity, and solvents. However, it cannot be eliminated due to the physical nature of the spin-coating process. In fact, iso/dense bias is a term that is used very loosely. Factors that affect the bias value include via size and via depth, density difference between the dense and iso areas, and their arrangement on the wafer. Therefore it is possible for one gap-fill material to exhibit quite different bias performance when it is used on differently patterned substrates. Nevertheless, the iso/dense bias can be approximated as proportional to the total via volume difference between iso and dense areas of the same size. Assuming that the bias is solely caused by volume difference, namely by distributing the same amount of material to two via fields having the same field area (S) but different via duty ratios (C_1 and C_2), the relationship of the film thickness (H) on top of the two via areas can be described as follows:

$$SH_1 + \left(\frac{C_1\sqrt{S}}{d}\right)^2 h\pi\frac{d^2}{4} = SH_2 + \left(\frac{C_2\sqrt{S}}{d}\right)^2 h\pi\frac{d^2}{4}$$

$$H_2 - H_1 = \frac{\pi h}{4}\left(C_1^{\,2} - C_2^{\,2}\right)$$

where h and d are via depth and via diameter, respectively. The value of $(H_2 - H_1)/h$ can be regarded as the reduction ratio (R) of the via-fill process. This is a very crude approximation, but it does reflect the basic relation between bias and volume difference.

In the worst case, the bias $H_2 - H_1$ is kept unchanged during the wet etch-back to the wafer top. Because a layer of anti-reflective coating will be coated, a similar reduction ratio will be applied. Therefore the final bias is proportional to R^2 and is usually well below the bias requirement.

The properties of the gap-fill material can also play an important role in bias reduction. Figure 8 shows the cross-sections of vias coated with EXP05013 before and after the wet etch-back process. The wet etch-back rate for this material is slower inside of the via than in the bulk film, allowing for the material above the isolated vias to "catch up" to dense regions in which the film has already developed back to the via. This unique property effectively reduces iso/dense bias.

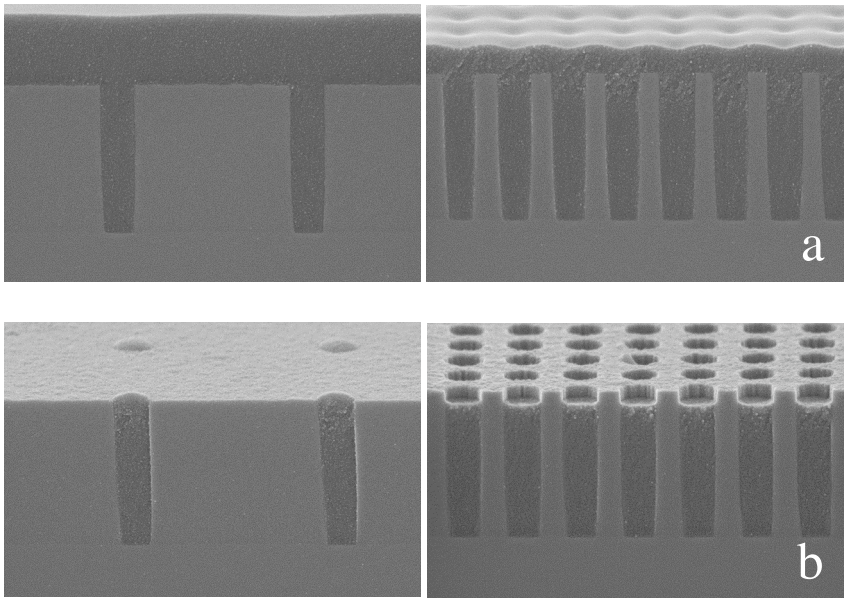

Figure 8. Wet etch-back performance of EXP05013 on IMEC silicon dioxide wafers (a) before and (b) after wet etch-back (220-nm via diameter, 1000-nm depth, 1:2 dense area duty ratio, and 1:6 iso area duty ratio).

3.4 Dry etch rate

In the trench etch process, the dry etch rate of the gap-fill material is an important process parameter. As linewidth decreases, the budget of resist thickness becomes even smaller, which in turn requires gap-fill materials to have faster dry etch rates to ensure adequate pattern transfer. Furthermore, the DD process requires the gap-fill material to have an etch rate similar to the low-k material in order to reduce fencing or crowning effects. One of the characteristics of the DD process is the large variety of process schemes in which it is applied at different wafer fabs. Consequently, materials of different etch rates are needed, although, in general, materials having higher etch rates are preferred as lines become smaller. Figure 9 presents the comparison of the etch rates of different gap-fill materials currently under development at Brewer Science. The reference used is ARC®29A.

4. CONCLUSION

Experimental wet etch-back gap-fill materials developed in at Brewer Science offer improved via fill and iso/dense bias reduction, wide process windows, and adequate dry etch rates. Therefore a wet etch-back gap-fill DD process may

provide a better alternative to the currently used dry etch-back gap-fill process to achieve planar surfaces required for trench lithography. The wet etch-back gap-fill process allows coating, baking, and etch-back to be done in the same track, which eliminates the need to transfer wafers between the etch and photo bays, which increases throughput, reduces defects, and makes the process more cost-effective.

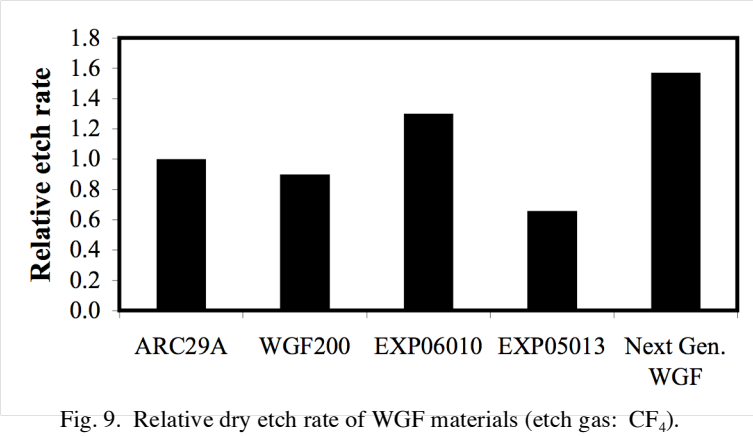

Fig. 9. Relative dry etch rate of WGF materials (etch gas: CF_4).

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