Wet-recess process optimization of a developer-soluble gap-fill material for planarization of trenches in trench-first dual damascene process

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ABSTRACT

This paper describes a new approach to help overcome the challenges of fabricating leading-edge devices by using the trench first dual damascene process. Wet gap-fill materials are designed to reduce film thickness bias across a wafer while keeping wafers in the same track in which they were coated. As the first process step, the wafer is coated with a thick layer of wet gap-fill material to fill all trenches, thus guarding against resist pooling in the trenches. The substrate is then baked to partially cure the wet gap-fill material. Standard 0.26N tetramethylammonium hydroxide (TMAH) is then used to wet etch the wet gap-fill layer back to the substrate surface. For this study, substrates with different trench depths and widths were processed, cross-sectioned, and measured. The effect of trench dimensions and aspect ratio on the develop properties of WGF200-343 was investigated to see if it could be used as a wet trench-fill material. This work will help develop a process that will allow the use of trench-first DD processing in modern semiconductor manufacturing.

Keywords: wet gap fill (WGF), dual damascene (DD), bias, trench-first, low-k

INTRODUCTION

Leading-edge devices require several copper interconnect levels, which has resulted in the widespread use of via-first and trench-first dual damascene (DD) processing. The via-first DD process has been widely implemented by the industry to address the smaller critical dimensions (CDs) of current devices and the inability to etch copper. With the transition to low-k dielectrics, new challenges have emerged. The 45-nm node is fast approaching, and new device designs utilizing unique structures and low-k dielectrics have emerged as a result. These designs necessitate new materials, such as wet gap-fill (WGF) materials, and novel-processing techniques, such as wet recess, to reliably and constantly manufacture devices. The via-first DD approach can leave organic residue in the bottom of the via after the trench is etched. This residue could be absorbed into the pores of the low-k dielectric and change the dielectric's properties.[1] This challenge has led to renewed interest in trench-first DD processing.

The traditional drawback to trench-first DD processing was the pooling of resist in the trenches where vias need to be patterned.[2] Using a gap-filling material to fill the trench and planarize the surface solves this problem. One approach to solve the problem is to use a dry-etch gap-fill material.[3] The drawback to a dry-etch gap-fill material is that it requires an additional etch step, which necessitates transferring the wafer lot to the etch bay. A WGF material would allow the wafer lot to stay in the litho bay, and in most cases, on the same coater/developer track.[4] This process feature would increase throughput over that used in the dry-etch gap-fill approach. Figure 1 shows the steps in the proposed process using a WGF material. First the trench is etched. Then the WGF material is spin coated over the wafer and then baked. Next the wafer is developed to remove the excess WGF. BARC and resist are then coated. A wet-developable BARC can be used in this step to increase the via etch budget. The vias are patterned in a microlithography step, and the resulting pattern is transferred to the substrate. Because the vias are etched last in the trench-first DD process, there is no possibility for residue. After cleaning, copper can be deposited.

The trench-fist approach to the DD process eliminates the possibility of residue left in the vias because the vias are the last features etched before copper deposition. By incorporating a WGF material into the trench-first approach, the process would be able to be used in modern semiconductor manufacturing. Additionally, the entire process would stay in the litho bay until via etching.

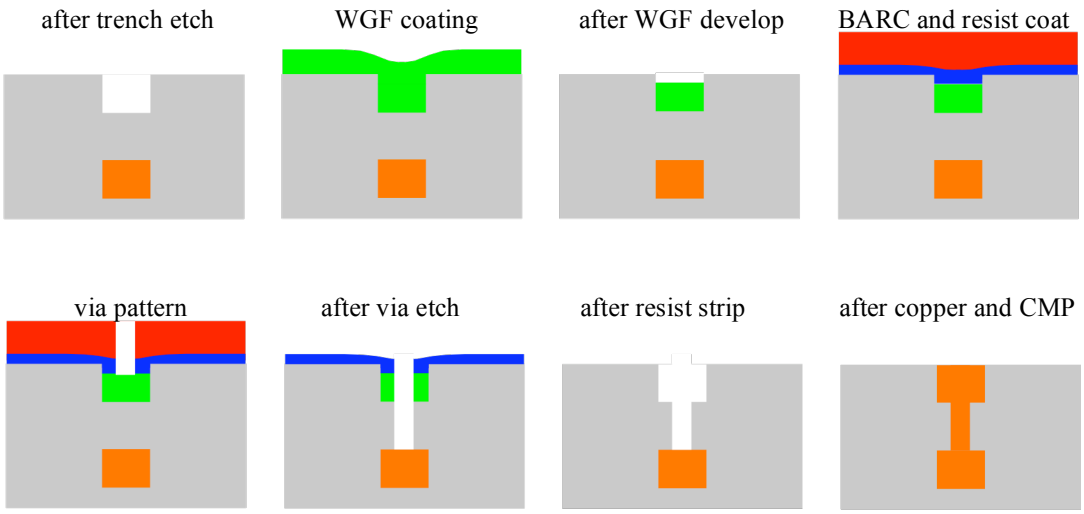


Figure 1. Trench first DD process using a WGF material to fill the trenches.

EXPERIMENTAL

Three separate tests were performed during this study, all at 60-second bake times. The first set varied bake temperature and develop time on three different substrates. The second and third sets varied only bake temperature with the develop time locked at 60 seconds. The processing conditions are listed in Table 1. The substrates were silicon with existing SiO_2 topography; details are listed in Table 2. The substrates were manually spin coated and contact baked on a CB100 coater/hot plate system. Developing was also manually processed on a CB100 using PD523AD 0.26N TMAH developer.

Substrate 1	
Bake Temperatures (°C)	Develop Times (sec)
160	30
165	45
170	60

Substrate 2	
Bake Temperatures (°C)	Develop Time (sec)
165	60
170	
175	

Substrate 3	
Bake Temperatures (°C)	Develop Time (sec)
165	60
170	
175	
180	
185	

Table 1. Processing conditions.

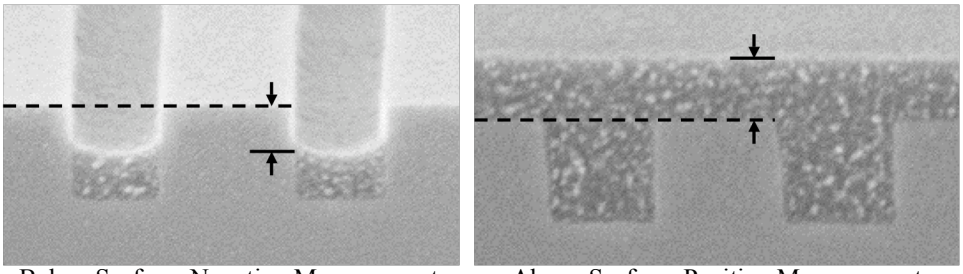
Substrate #	Feature Depth (nm)	Feature Width (nm)	Aspect Ratio
1	200	220	1:1.1
1	200	500	1:2.5
2	500	220	2.3:1
2	500	500	1:1
3	200	600	1:3
3	200	800	1:4
3	200	1000	1:5

Table 2. Substrate feature sizes.

RESULTS AND DISCUSSION

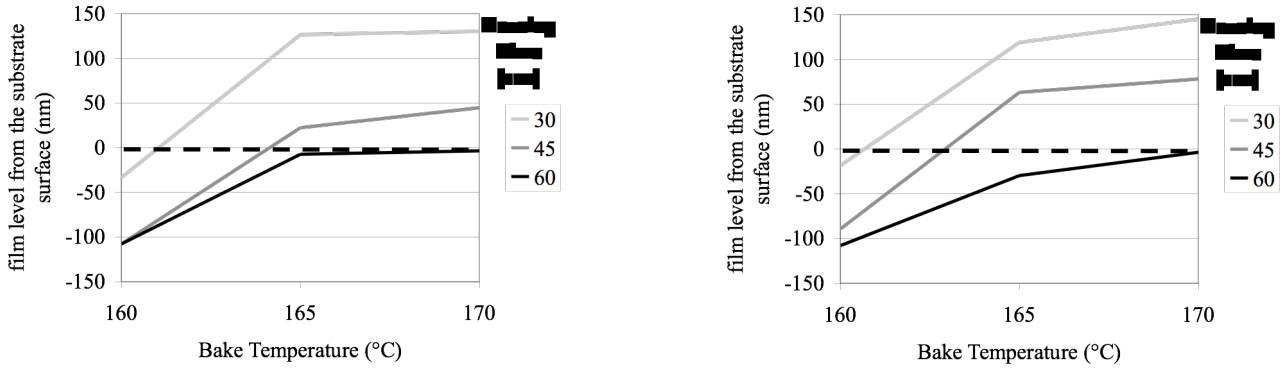
Figure 2 explains the measurement conventions used in measuring the substrates and plotting the data. When the film was below the surface, shown by the dashed line, the measurements were negative. When the film was above the surface, again shown by the dashed line, the measurements were positive.

Figure 3 shows the thickness of WGF200-343 after development. The dashed line in the plot marks the location of surface; the same as in figure 1. It can be seen in figure 2a and 2b that below 165°C, the level of WGF200-343 decreases more then above 165°C for a set bake time and develop time. Thus the rate of development of WGF200-343 is faster below 165°C then above it, and above 165° the develop rate levels off. This is the same response from WGF200-343 when tested on plain Si wafers[3].



Below Surface, Negative Measurement Above Surface, Positive Measurement

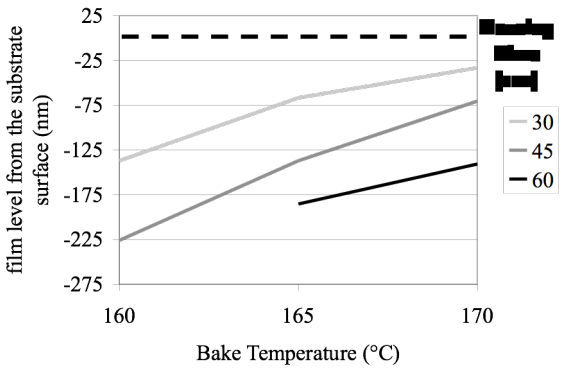
Figure 2. Measurement conventions of substrates.



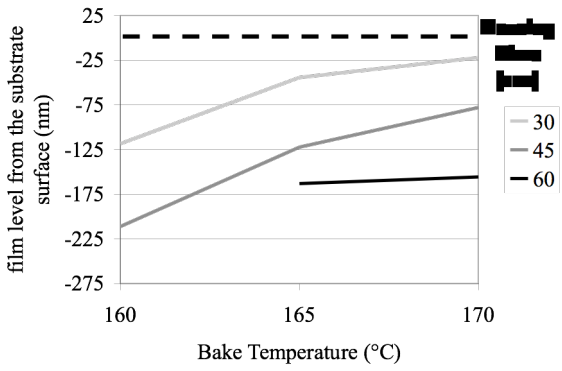
a. Depth: 200 nm; width: 220 nm b. Depth: 200 nm; width: 500 nm

Figure 3. Trench fill, substrate 1.

In Figure 3a the aspect ratio is 1:1.1, and in 3b the aspect ratio is 1:2.5. The film level is similar across bake temperature and develop time for the two different aspect ratios. This trend is also shown in Figure 4a and 4b. The aspect ratio in Figure 4a is 2:1, and in 4b it is 1:1. Again the film level is similar for the two different aspect ratios. Conversely, when Figures 3 and 4 are compared, a large difference is seen. Even though both substrates are SiO_2 topography over Si and the widths of Figures 3a and 4a, as well as those of 3b and 4b, are the same, the depths of the trenches are different. Figure 5 combines the 45-second develop plots of substrates 1 and 2 (Figures 3 and 4). It can be seen that the difference in the film level after development comes from the difference in trench depth. This is supported by substrate 3 shown in Figure 6. A single develop time was used, but three different aspect ratios are shown (1:3, 1:4, and 1:5), and all have similar develop characteristics across all trench widths. This trend is believed to come from differences in initial thickness of WGF200-343 from coating over trenches with different depths. This could be easily be adjusted by a change in processing or formulation. A change in spin speed to produce a change in initial thickness to account for the difference in trench depth, or an adjustment to the percent solids of the formulation could also change the initial thickness.



a. Depth: 500 nm; width: 250 nm



b. Depth: 500 nm; width: 500 nm

Figure 4. Trench fill, substrate 2.

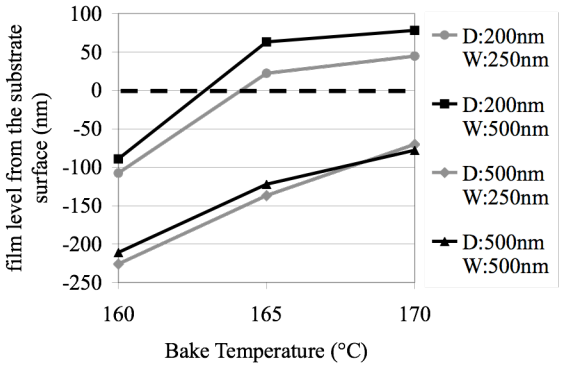


Figure 5. Combination of substrates 1 and 2, 45-second develop time.

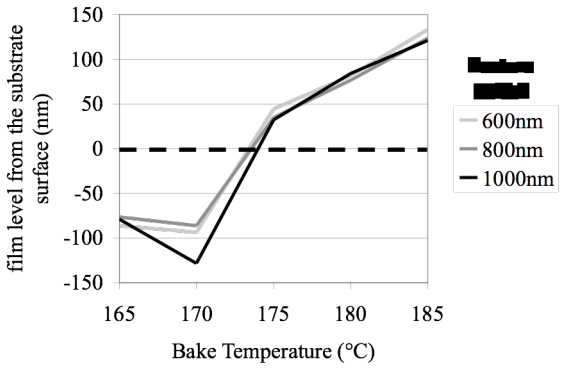
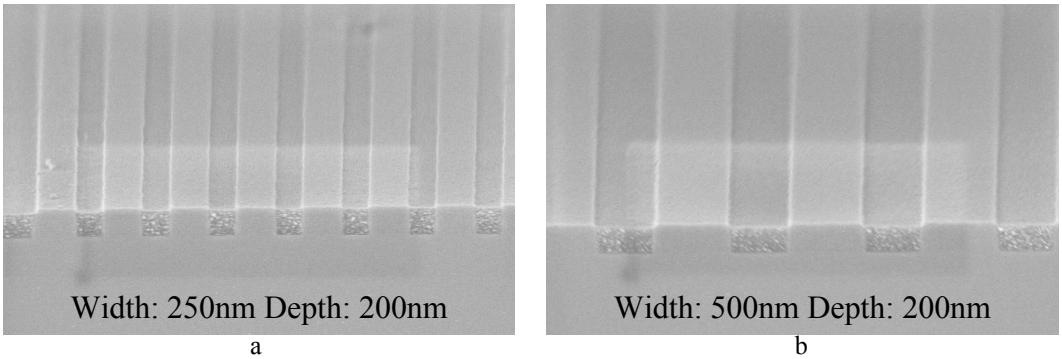


Figure 6. Trench fill, substrate 3, depth: 200 nm.

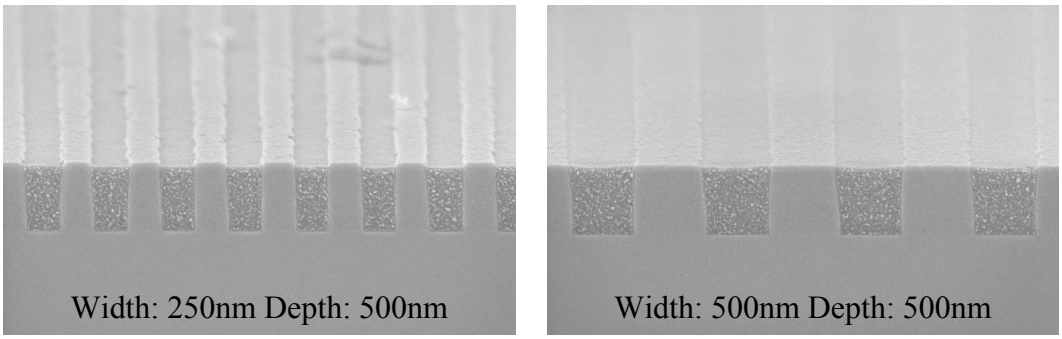
Figures 7 and 8 show SEM cross-sections of substrates 1 and 2, respectively. As the trench width changes, for the same processing conditions, WGF200-343 fill is similar. The fill is also flat with no visual meniscus. Figure 10 shows the cross-sections of the measurements of substrate 3. The WGF200-343 in these trenches was overdeveloped. Even in this extreme case of a low aspect ratio and an overdeveloped film, the WGF200-343 shows a flat profile with no curvature, except at the very edge. To achieve full fill in these trenches, a higher bake temperature or shorter develop

time would need to be used. Conversely, Figures 9 and 10 show a slight curvature of the WGF200-343. These cases of narrow trenches and overdevelopment may show the limit of this process. However, further testing with BARC and resist coatings is needed to determine the certainty of this limit.



a b

Figure 7. Cross-sections of substrate 1, 165°C bake, 60-second develop.



a b

Figure 8. Cross-sections of substrate 2, 170°C bake, 30-second develop.

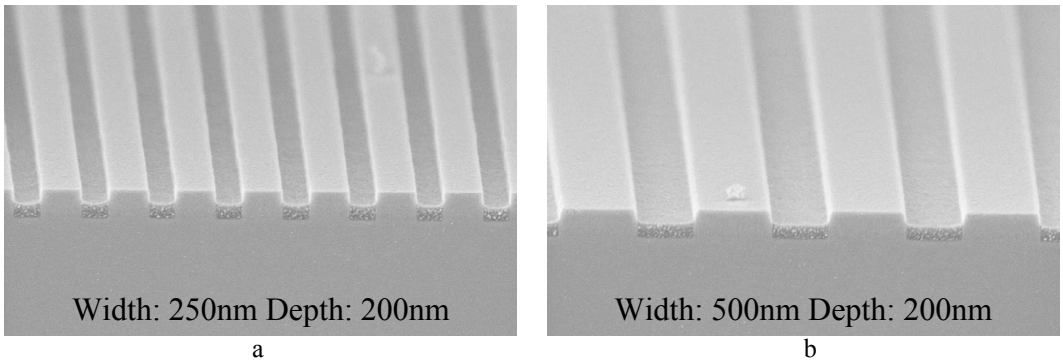


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Figure 9. Cross-sections of substrate 1, 160°C bake, 60-second develop.

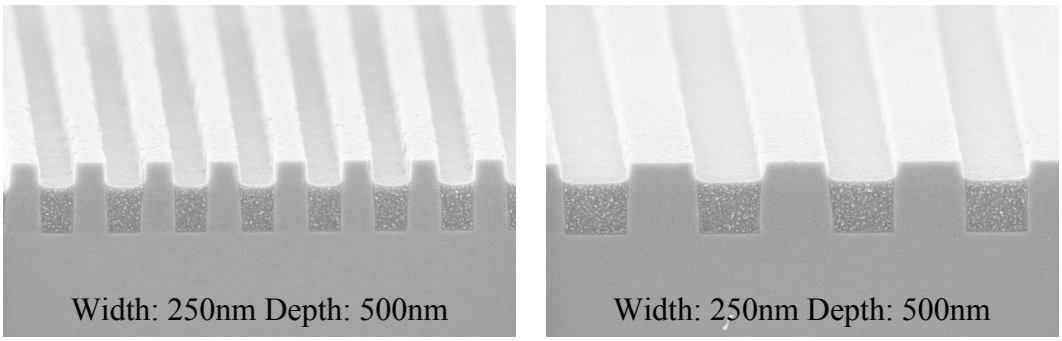

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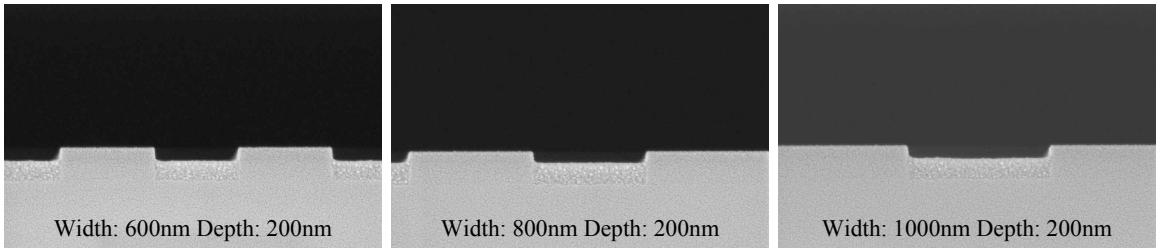
Figure 10. Cross-sections of substrate 2, 165°C bake, 60-second develop.



a b c

Figure 11. Cross-sections of substrate 3, 165°C bake, 60-second develop.

CONCLUSIONS

In summary, WGF200-343 can be used to fill trenches with a variety of widths and depths. It was also shown that the aspect ratio of the trenches had little to no effect on the develop characteristics of WGF200-343. Instead, the trench depth was a major factor in affecting how much material would be left in the trench after the develop step. The post develop film inside of the trenches was flat in most cases, excluding the partial fill of substrates 1 and 2. Further work investigating how BARC and resist will coat, and ultimately a via patterning comparison against a process of record will need to be undertaken to prove out this process.

ACKNOWLEDGMENTS

The authors would like to thank John Thompson and Denise Howard for their diligent SEM work.

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