

# High-resolution defect metrology for silicon BARC analysis

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## ABSTRACT

Measuring coating defects on two or more blanket film layers is difficult and can be misleading due to reflectivity changes from the bottom layer, and surface roughness not present when the substrate is only polished silicon. To improve signal-to-noise ratio and establish a lower limit for particle size detection, polystyrene latex (PSL) spheres are deposited on the film stack. Particles as small as 54 nm were detectable on a stack 330-nm thick using a Hitachi LS Series Surface Scanning Inspection System (SSIS) and RS5500 Defect Review Scanning Electron Microscope (DRSEM). These systems have advanced capabilities enabling automated detection, classification, and characterization of defects down to 30 nm or smaller on some substrates and films. Haze wafer maps are related to surface roughness and reflectivity and show unusual asymmetries possibly caused by dispense problems or exhaust flow patterns during baking. These maps can be helpful to find problems in the coating system, even if film thickness is on target. Preliminary testing results are presented for a typical trilayer pattern stack for high-resolution 193-nm patterning consisting of a silicon spin-on hardmask (HM) layer on top of a spin-on carbon (SOC) layer. The majority of the defects were caused by bubble formation within the HM that was modulated by process conditions used for these tests. A higher spin speed for the HM coating produced lower defects, most likely due to a thinner film with less trapped solvent during baking, but this effect will require more study, as it could also be due to a faster evaporation rate caused by higher airflow. Pre-wet, spin time, and bake temperature did not produce significant effects within these tests, but showed trends requiring further study. These advanced spin-on HM materials can be applied as thin as 15 to 20 nm due to their high etch selectivity. With the use of such high-resolution defect metrology, very subtle chemical interactions and process effects can be examined to find the ideal process conditions for both the SOC and HM layers.

## 1. INTRODUCTION

The purpose of this study is to explore the limits of defect detection and classification capability on blanket multilayer patterning films with state-of-the-art equipment designed for the 32nm manufacturing technology node. In the transition from single-layer pattern stacks to dual-layer (anti-reflective coating+resist) stacks, the number and types of defects increases. Some defects unique to bottom anti-reflective coatings (BARC) layers are caused by the cross-linking used to render the films impervious to resist solvents. BARC layers are also generally thinner than photoresist layers, a fact that reduces the probability of particles but also leads to other defect mechanisms such as pinholes. The early part of the last decade saw the mainstream introduction of trilayer patterning stacks.<sup>1,2,3,4,5</sup> A common approach is to deposit a thick, planarizing layer of material resistant to etching of the substrate, followed by a thinner layer of material that etches faster than photoresist, but much slower than the planarizing layer. In this way, a very thin, fragile ArF photoresist can be used to pattern the thinner layer, and the high selectivity between the middle and bottom layers permits pattern transfer to the substrate with high fidelity to the original photoresist pattern dimensions. This approach has allowed resists with relatively poor etch resistance to be used for pattern transfer into very thick substrates such as trench oxides for interconnect layers. One result of this trilayer approach is the further increased opportunity for defects, whether they are killer defects that can cause localized defocus or blocked etch, or nuisance defects that prevent detection of defects in other layers. However, the reduction of systematic optics-related defects due to superior planarization and reduced reflectivity can easily compensate and make trilayer patterning an attractive approach. Spin-on coatings allow the entire stack to be deposited in a short time within similar coating equipment – even the same coating track – without the need for more costly CVD tools or other forms of vacuum deposition.

In the ever-increasing struggle to find significant defects, measurement instrument sophistication has grown to the point where 30-nm defects are now detectable, while 20-nm defects can cause shorts or opens due to the small pattern pitch. State-of-the-art filters for manufacturing and dispensing lithographic films such as BARCs and photoresists have pore sizes in the 10-nm range, although capture efficiency is often as much a function of media type as filter pore size itself.<sup>6,7,8</sup> Stage accuracy within the Surface Scanning Inspection System (SSIS) and Defect Review Scanning Electron

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Microscope (DRSEM) systems used for this investigation permits reliable location of defects for review and classification. These capabilities allow today's yield engineers to quickly sort through vast numbers of defects and identify root causes through a semi-automated system of classification that points to the mechanisms of formation of the defects. A common sampling methodology is to run bare silicon wafers with a single film layer to isolate the defects from a coating process.<sup>9</sup> This method is helpful to monitor the performance of a BARC or resist product, track system, spin-coater, and bake plate module on a periodic basis. In some cases these single-layer monitor results may correlate to defects detected on the patterned wafers after the develop step or after etching, but for the most part they provide an early warning system for any coating issues before they become a threat to the patterned wafers. As the intensity of reflected light from the laser probe is a function of the film coated on these wafers, special calibration is often necessary to account for the specific films respective refractive index under evaluation. Calibration consists of depositing polystyrene latex spheres (PSLs) on a wafer coated with the BARC or resist layer, and scanning these spheres to determine the detector peak area to particle size relationship, and the background noise level.<sup>10</sup> In practice most defects do not resemble PSLs, but this method of calibration is still an effective way to screen point defects for rough sizing before classification.

For this investigation trilayer film stacks, without the photoresist, are examined after calibration by the PSL method. The bottom layer, which is unchanged within each test, is a highly crosslinked aromatic polymer used as a low-defect spin-on carbon (SOC) layer, while the second layer is a silicon-based hardmask (HM) material. By scanning after both the SOC and HM layers are coated, a more accurate result is obtained than for single-layer films. This increased accuracy is due the fact that surface energy plays an important role in the wettability and drying rate of the HM layer. Several defect types have been classified and compared for different coating conditions. Follow-up studies are planned to study these defect mechanisms and the sensitivity afforded by different BARC, HM, and SOC types. By using several detectors to view defects from different angles it is possible to see the formation mechanisms unfold as they are frozen in the film during the drying process. For example, a bubble appears either as a bump or as a crater or pit depending on when drying occurred. Pieces of burst bubbles can also redeposit as particles nearby. Through a process of coating recipe improvement, such defects can be eliminated.

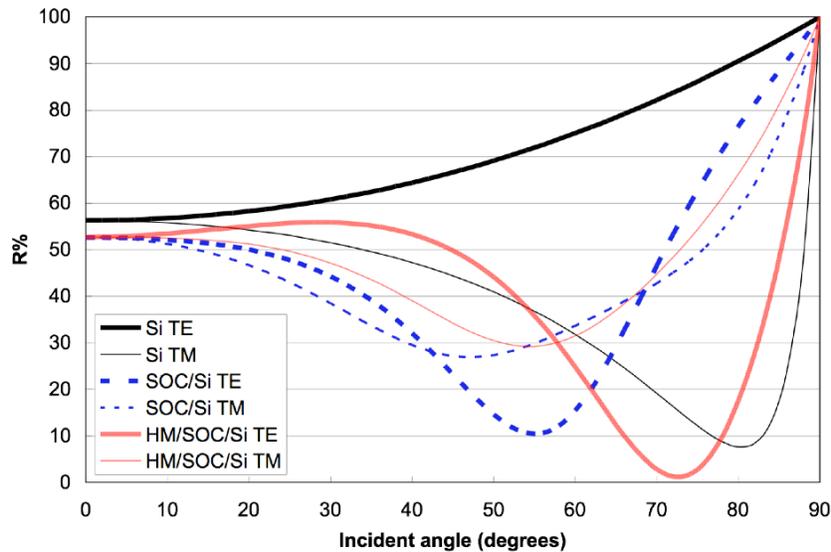
## 2. EQUIPMENT AND STUDY DESIGN

Coating defects were examined on 300-mm blanket-coated wafers in two separate screening tests. The coating factors for this study were applied to the top HM layer, while the bottom SOC layer was coated the same for all runs within each test. Factors included having the pre-wet step on or off, changing the casting spin speed from 1500 to 2500 rpm, spin time from 8 to 300 seconds, and bake temperature from 165 to 240°C, as shown in Table 1. The baseline condition for this stack is also given in the right-most column of the table. The SOC layer was deposited with a volume of 1.5 ml, a dispense spin speed of 3000 rpm, a casting spin speed of 1500 rpm, a casting time of 30 seconds, and a bake of 205°C for 60 seconds. The substrates were defect-grade p-type (boron) 300-mm bare silicon wafers, with <100> silicon and <110> notch orientation, specified to have 100 or less localized light scatterers at 0.12 μm by the manufacturer. For the first test the SOC layer was coated on a TEL Lithius track, while for the second test a Sokudo RF<sup>3</sup> track was used to coat the SOC layer. In both tests a TEL Lithius track was used for the HM layer, and various recipes were created to adjust the parameters of the HM coating study in each test. Coating conditions included a dispense spin speed of 3000 rpm and dispense time of 3.5 seconds. Spin time in the second test consisted of 12 seconds casting time, followed by an extended drying time totaling from 60 to 300 seconds, to exaggerate the effect of drying time. Overall, defect levels for the second test were lower than the first, but this could be due to equipment variation or other uncontrolled factors. To eliminate as many nuisance defects as possible, and focus on material/process interactions, a relatively large dispense volume of 3 ml was used for the HM. In actual use, the dispense volume can be much lower.

**Table 1.** HM layer factors and levels used in defect tests.

<i>Factor</i>	<i>Test1</i>	<i>Test2</i>	<i>Baseline Condition</i>
Pre-wet	On	On/Off	On
Spin Speed (rpm)	1500-2500	1500-2500	1500
Spin Time (sec)	8-60	60-300	60
Bake Temp (°C)	205	165-240	205

Defect inspection and analysis were performed using a Hitachi LS Series SSIS and RS5500 DRSEM. The probe wavelength is less than 400 nm for high-resolution defect detection on the LS Series. These systems have advanced capabilities enabling automated detection, classification, and characterization of defects down to 30 nm or below on some substrates and films. Haze maps are related to surface roughness and localized reflectivity and show unusual asymmetries possibly caused by exhaust flow patterns during baking. These maps can be helpful to find problems in the coating system, even if film thickness is on target. Specialized computer hardware is available to process haze data with this equipment. The reflectivity of the film stack at the probe wavelength is generally lower than bare silicon, as shown in Figure 1 for a range of incident angles covering a range of possible detector positions. For transverse magnetic (TM) polarization the coated wafers have higher reflectivity than bare silicon only for incident angles higher than 60 degrees.



**Figure 1.** Reflectivity comparison of bare Si, SOC/Si, and HM/SOC/Si film stacks at the scanning probe wavelength for both transverse electric (TE) and transverse magnetic (TM) polarizations.

### 3. RESULTS

The process of defect testing begins with PSL calibration on the two-layer film stack, consisting of HM with thickness of 30 nm applied at the nominal spin speed of 1500 rpm on top of a 300-nm SOC layer. In addition, PSL calibration was performed for the HM at the higher spin speed of 2500 rpm, corresponding to a thickness of 22 nm, for the SOC alone, and for the bare silicon case. There were 11 circular regions deposited with nominal PSL sizes of 33, 40, 46, 60, 73, 81, 97, 151, 199, 299, and 499 nm. Approximately 1000 particles were electrostatically deposited within each circle. Each population has a sizing spread of approximately 5 nm, as shown in Figure 2. The wafer maps in all four cases, given in Figure 3, clearly show which spheres were resolved and their size distributions. The smallest particles were at the 5 o'clock position, and particle size increased counterclockwise around the wafer. For bare silicon, all circles appear in the scan, and the minimum detected size was 32 nm. As seen in Figure 3 there are a large number – approximately 2000 – background defects even for the bare silicon case of Figure 3(a) when viewed at this resolution, as compared to the usual background of less than 10 defects observed with less sensitive metrology equipment. A higher grade of defect testing wafers such as interstitial-rich or epitaxial silicon wafers is required to reduce the background noise at this very high resolution. Nevertheless, useful information for improving the coating process was obtained. For HM coated at 1500 rpm in Figure 3(c) the first two circles are not resolved and the smallest detected particles measured 56 nm. For HM coated at 2500 rpm, Figure 3(d), the minimum size was slightly lower, at 54 nm. With SOC alone, Figure 3(b), the minimum detected PSL was also 54 nm. Thus, the reflectivity of the stack, combined with the background noise and haze, has an effect on the sensitivity of detection.

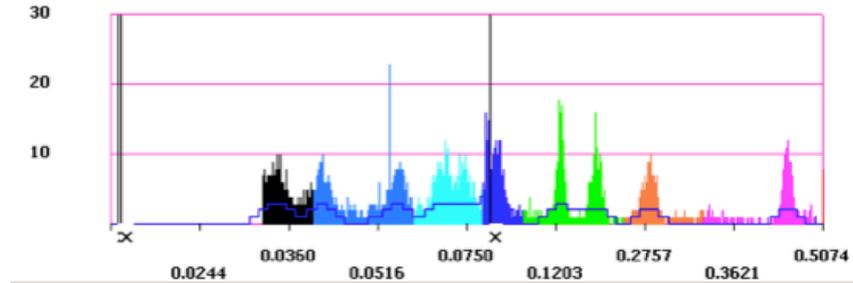


Figure 2. Histograms of PSL regions on bare silicon.

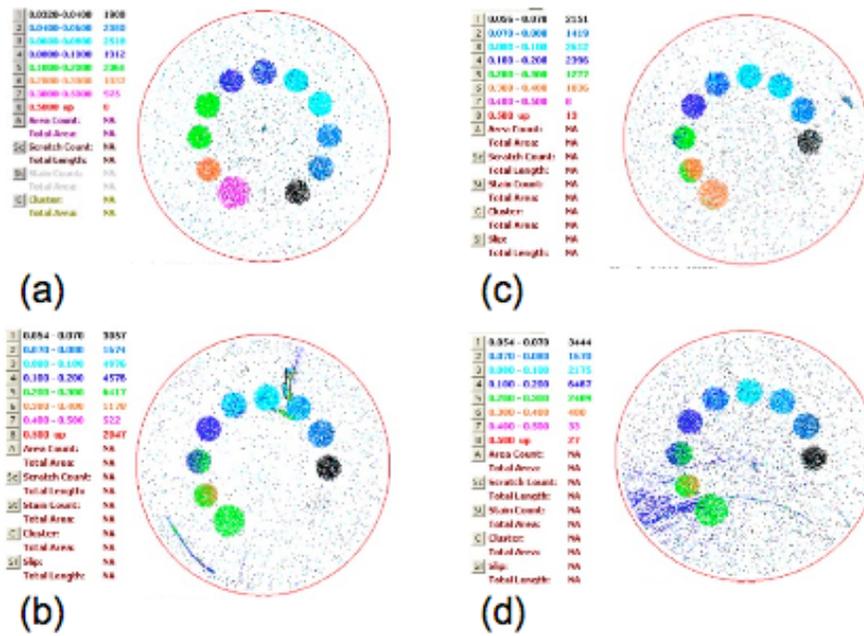
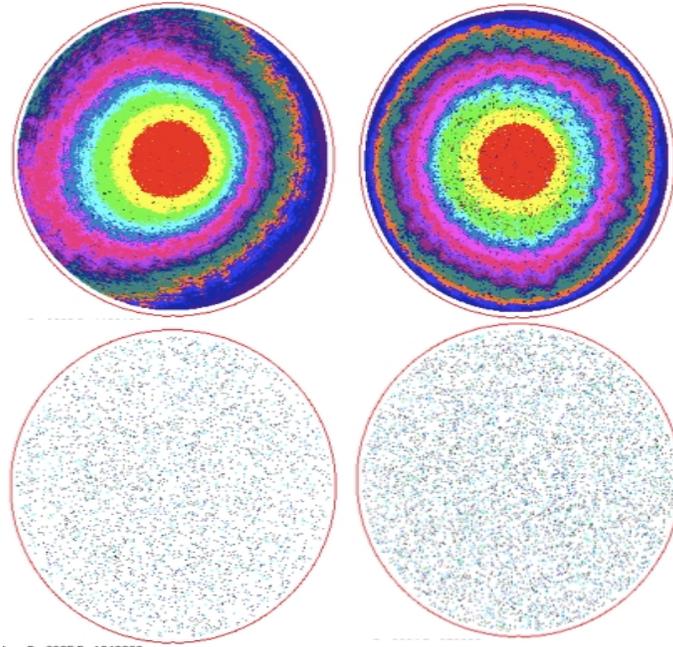


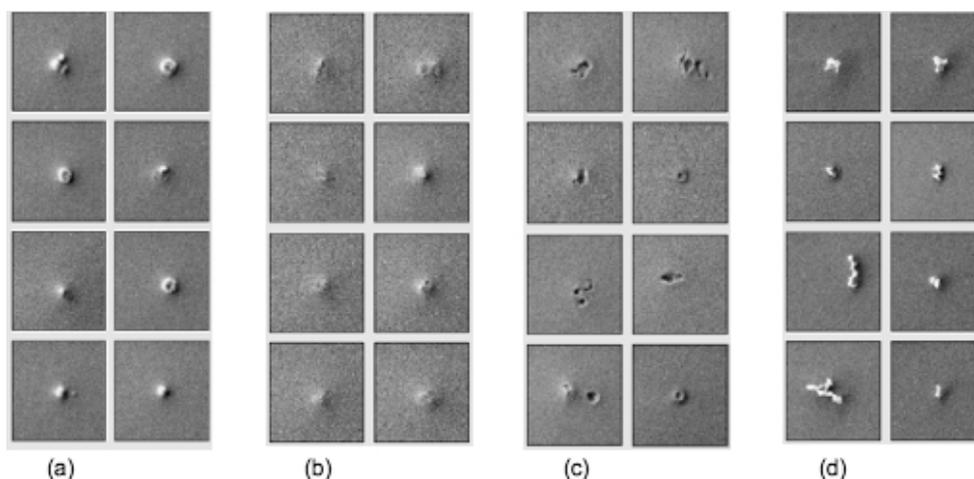
Figure 3. PSL maps for four different film stacks: (a) bare silicon, (b) SOC only, (c) HM at 1500 rpm, and (d) HM at 2500 rpm.

Haze results from this study were erratic and warrant further study. Some maps show the expected radially symmetric pattern, while others are radial with an offset to one side. None of the scans of the SOC layer alone show these offset patterns. No correlation exists between haze symmetry and defect counts or specific defect types. The purpose of emphasizing these maps is to highlight the sensitivity of the LS Series tool to slight surface roughness and reflectivity effects that do not show up in the point defect maps, all of which are completely random and have no radial signature. The haze results for two wafers having the exact same coating conditions, that is, spin speed of 1500 rpm, spin time of 60 seconds, and bake of 240°C, are shown in Figure 4. The map on the left is asymmetric, and the one on the right is symmetric. One hypothesis for the offset maps is that these wafers were baked with an off-center exhaust flow in the bake plate chamber. Another hypothesis is that the dispense nozzle was offset to one side in a manner that varied from wafer to wafer. To better understand this effect, further tests are planned, including tests with no bake or with bake exhaust adjusted. Sensitive haze inspection can thus show subtle problems with the coating system that would not be readily apparent using thickness metrology or point defects alone.

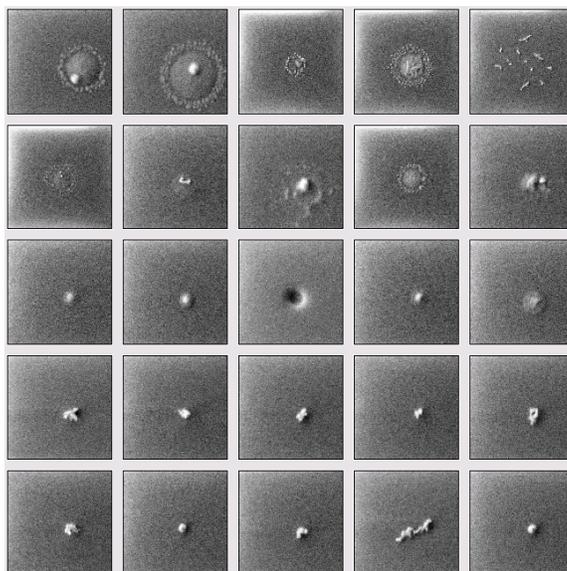


**Figure 4.** Haze maps (top) and particle maps (bottom) for HM/SOC stacks coated with the HM conditions of no prewet, casting speed and time of 1500 rpm for 60 seconds, and 240°C bake.

Classification of the defects from the HM/SOC stack revealed that almost all of them arose from a single mechanism, namely, bubble formation caused by these coating conditions. Results for this stack vary from tool to tool and process to process. At least two wafers were run at each process condition, and in most cases three wafers. Example images from the DRSEM review are shown in Figure 5. The majority of defects (62% on average) were small bumps, some examples of which are shown in the RS5500 review images in Figure 5(b). The next most numerous were fall-on particles (23%) shown in Figure 5(d) that in many cases appear to be the remnants of burst bubbles that formed during the coating and baking step due to residual solvent in the film. Bubbles were visible in various forms as shown in Figure 5(a), where they appear as a round crater-like structure making up 8.7% of all defects, and as crater-like pits in Figure 5(c), at 3% of total. The rest are unclassified. As measured by the RS5500 these defects range in size from about 70 to 200 nm, but some crater features are as small as 40 nm. No obvious bubble-type defects appeared on the wafers coated with SOC alone. The defects found on the SOC-coated wafers were drying-related circular defects commonly observed for organic materials such as BARC and resist, or fall-on particles. Some example images from the SOC layer review are given in Figure 6. These ranged in size from about 70 to 500 nm. More studies with these advanced inspection tools will be needed to determine if any of these types of defects are observed for a single layer of HM alone, or without the bake step applied.



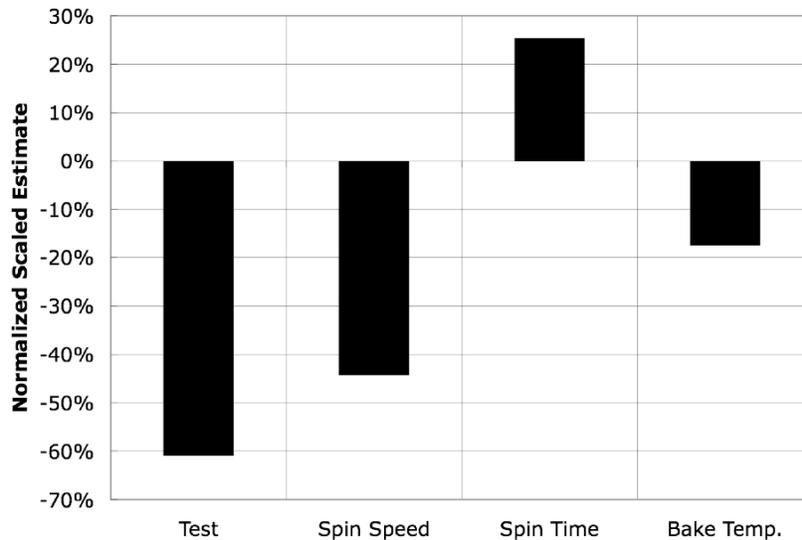
**Figure 5.** Defect types from classification including (a) bubbles, (b) bumps, (c) craters, and (d) fall on particles. The field of view for these images ranges from 0.88 to 1.1  $\mu\text{m}$ . The defects are 70 to 200 nm in size, with some smaller features visible as well. The smallest crater features are 40 nm in size.



**Figure 6.** Defect review images for the SOC layer alone, also with an image field of view ranging from 0.88 to 1.1  $\mu\text{m}$ . The defects ranged in size from 70 to 500 nm.

Factor effects from these two tests are presented as normalized estimates in the chart of Figure 7. Pre-wet had no significant effect on defect counts in this study, and is thus omitted from the chart. Overall, bubble-related defects varied from test to test, possibly due to the SOC coating differences or other uncontrolled factors, making the test variable the largest single factor effect. The next largest factor effect was for spin speed, which caused a 44% reduction in defects going from 1500 to 2500 rpm. The difference in HM thickness in going from 1500 to 2500 rpm, as mentioned above, is from 30 to 22 nm. A thinner film has less volume for trapped solvent, but other factors may also be coming in to play with spin speed. Follow-up studies are planned to look at the effect of spin speed independently of thickness. Spin time is the next largest factor effect, although not statistically significant, causing about 25% more defects at 300 seconds than at 60 seconds. This was surprising, as the effect of spin time should be to increase the drying of the film while under the higher airflow due to rotational speed, thus reducing the trapped solvent at the bake step. Similar factors, such as a higher exhaust flow, or a slower two-stage bake to improve drying, have been examined in prior studies, but these drying

factors showed mixed results, both increasing and decreasing defect results in different tests. Finally, the bake temperature effect is to decrease defects 17% going from 205 to 240°C, but was also statistically insignificant and varied from test to test. A reduced bake temperature should drive the solvent off more slowly and would be expected to reduce bubble-type defects. This HM/SOC stack permits HM layers as thin as 16 nm to be used with a good lithographic process window and sufficient etch resistance for etching the SOC layer completely in oxygen plasma.<sup>11</sup> Model predictions aside, the lowest defect counts for this study were achieved in the second test at a condition of 2000 rpm, 60 seconds, and 180°C bake, with a reduction of 56% in total defects from the baseline conditions of 1500 rpm, 60 seconds, and 205°C. Further process optimization is expected to completely eliminate these defects with this process/track system.



**Figure 7.** Normalized scaled estimates of the defect response for the experimental factors. Pre-wet is excluded because it showed almost no effect.

#### 4. CONCLUSION

This preliminary series of tests has provided a framework for future defect studies to improve the coating process for low-defect coatings on multilayer stacks of blanket films. The high sensitivity and resolution of the Hitachi LS Series defect scan and RS5500 SEM review enables very subtle coating effects to be quickly and easily located and classified. In this particular case, several defect types were classified according to a single mechanism that could be related to drying. Also, inconsistent asymmetry in haze maps indicates a problem with the coating/baking system that would be of concern in manufacturing. Such analysis would be helpful for many types of film stacks, including resist/BARC, gap-fill/BARC, resist/topcoat, resist/TARC, or other cases. The Hitachi LS Series provides approximately 50-nm size resolution for defects on these HM/SOC film stacks, compared with 30-nm capability on bare silicon, and the RS5500 review allows a classification of defects at various stages of formation so that their common mechanism becomes apparent. Small changes in surface roughness or reflectivity apparent in the haze maps may be compared with other types of surface metrology to understand better the coating process and the interaction between film layers that makes this test more complex than single-layer evaluations. The improved sensitivity afforded by multilayer defect analysis should provide better capability for statistical control of process equipment, thus improving overall pattern yield.

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