Filling and Planarizing Deep Trenches with Polymeric Material for Through-Silicon Via Technology

R.K. Trichur, M. Fowler, J.W. McCutcheon, and M. Daily
Brewer Science, Inc.
2401 Brewer Drive
Rolla, MO 65401

Abstract

A key driver for 3-D device integration has been through-silicon via (TSV) technology that enables through-chip communication between vertically integrated layers. The TSVs typically have an electrical isolation using a dielectric layer between the silicon and the interconnect metal (e.g., copper). Recently, polymers have been proposed for use as the dielectric isolation layer, and polymers have been shown to increase device reliability by reducing "copper pumping," where copper pops out from the TSV holes during thermal cycling. Traditionally, spin- or spray-coating techniques have been used to fill TSVs with polymer material. However, using those techniques to fill and planarize very deep trenches (~ 400 µm) and high-aspect-ratio structures has many limitations and usually results in voids, nonplanar surfaces, and lack of polymer flow to the requisite depths. Here, we present a novel process and a tool to completely fill and planarize deep trenches with a polymeric material. We use a combination of a traditional spin-coating process together with a physical planarization and fill process using the contact planarization tool to evacuate the trenches or vias on the wafer and then force the polymeric material inside the features. Using this process, we successfully filled and planarized trenches and vias 180 µm deep with 50-µm wide patterns as well as 400-µm deep trenches with ~ 400-µm wide patterns. Initial results show complete filling and planarization of the material in the trenches without any voids.

Introduction

Three-dimensional (3-D) integration allows for smaller, faster, and more functional microelectronic devices. Consumer demands for multifunctional electronic gadgets with reduced form factor has driven 3-D integration for the past several years. Here, vertical integration of functional devices in a package using TSVs are practiced instead of in-plane 2-D integration or integration between 3-D layers using wire bonding of devices. TSVs are fabricated using a series of processes mainly involving wafer thinning, deep reactive ion etching, dielectric deposition, and electroplating. Recently, polymers have been used as dielectric layers in deep silicon vias[1,2,3] and have been shown to improve the reliability[1] of TSVs by reducing adverse impacts of thermal expansion mismatch between copper and silicon during temperature cycling of the fabricated TSV wafers. This process involves filling the polymer dielectric material through the high-aspect-ratio deep trenches and vias.

Previous work has demonstrated filling of vias using spray- [3] and spin-coating [4] methods. Although these methods are well-established fabrication processes, there are many disadvantages associated with either method. When the spray-coating method is used for trench/via fill, multiple coats must be applied to the wafer, resulting in increased processing time and low throughput. Also, the spray-coating process is usually limited to low-viscosity materials. The final features could contain small voids that are caused by air being trapped between the multiple sprays.

For a spin-coating process, the mechanics of spin coating are bound to trap air in deep vias and trenches, and spin coating seldom results in good fill or well-planarized structures. Although modifications of the polymers' viscous and rheological properties have resulted in better fill performance, non-planar structures still result at the top of the wafer. During the polymer etch-back process, the non-planarity of the filled polymer affects the underlying materials and via fill as the non-planarity is partially transferred to the wafer structures.

Due to these limitations, there is a need for a process that will provide void-free filling of deep trenches and vias with good planarity while maintaining a comparable throughput associated with other IC manufacturing processes. In this paper, we introduce a novel process for filling and planarizing deep via

and trench structures using a contact planarization* process.

Experimental

Two types of test structures were used for initial tests to demonstrate trench fill and planarization. The first test structure was a 180 µm tall, 50 µm wide trench created on a silicon wafer using a thick photoresist material (SU-8 2025). For this structure, the photoresist was coated on the wafer at 1000 rpm for 40 s, followed by a soft bake at 65ºC for 3 min and 100ºC for 3 min. Then another layer of photoresist was coated and baked using the same conditions to increase the height of the test structure to 180 µm. After the second soft bake, the wafers were exposed to a dose of 450 mJ/cm^2 using a broadband UV source. Following the UV exposure, a post-exposure bake was done at 65ºC for 4 min followed by 100ºC for 4 min. Then the wafers were cooled down on a chill plate to room temperature. The photoresist structures were developed using an immersion bath process using SU-8 developer followed by an isopropanol (IPA) and deionized (DI) water rinse. In this process, the wafers were immersed in an SU-8 developer bath for 5 min with agitation, followed by an immersion rinse in an IPA bath for 1 min and then a DI water rinse in a dump rinse tank. Then the wafers were spin dried in a spin rinse dryer. After drying, the photoresist was hard baked at 220ºC for 5 min to completely cure the structure.

The second test structure was created on a silicon wafer. This test structure has three different features spaced in close proximity to one another and spread across the entire 200 mm wafer. The first feature is a large trench that is 400 µm in depth and 500 µm in width. The second feature is a smaller trench with a depth of 100 µm which is 50 µm adjacent to the larger trench. The wafer also has positive topography structures that were ~ 25 µm tall and were formed using glass frit deposition. Thus, in this design, the trench fill and planarization must be done for a total peak-to-valley dimension of ~ 425 µm.

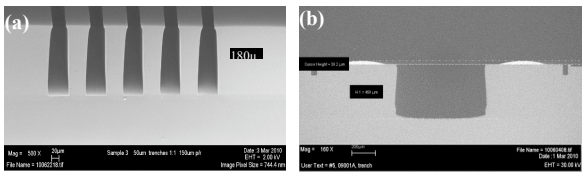

Figure 1. SEM image of two test structures created for contact planarization and trench-filling process demonstration: (a) 180 µm deep and 50 µm wide trenches created using thick photoresist on a silicon wafer; (b) 400 µm and 100 µm deep trench in silicon wafer with a 30 µm tall glass frit structure.

*CON-TACT® planarization developed by Brewer Science.

Figure 1 shows the cross section views of both test structures. Figure 1(a) shows the first structure type, which are trenches 180 µm tall and 50 µm wide. This structure type has a slight "T-topping" due to overexposure of the negative photoresist, resulting in a slightly reduced width of ~ 40 µm at the top of each trench.

If the 180 µm deep trench is coated with a photoresist using a standard spin-coating process, the coating will neither be able to get inside the trenches evenly nor planarize the topography after the spin-coating process. More than likely, it will create voids inside the trench features and non-planar topography on the surface after the spin-coating process. Wider trenches are easier to fill, but planarization is not achievable. Figure 2 illustrates the voiding and non-planarity experienced by coating a polymer material over the 180 µm deep topography. In this case, the same SU-8 material was coated on top of the SU-8 structures. Even with the similarity between the two materials, good coating and filling quality was not achieved.

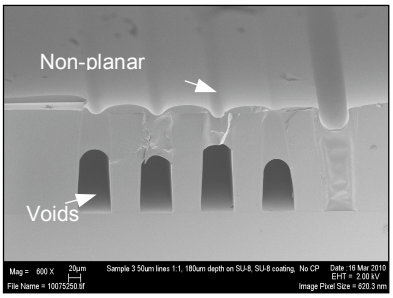

Figure 2. SEM image of spin coated trench feature showing the voids and non-planar surface commonly resulting from spin-coating processes for filling deep trenches or vias.

To address these issues with via filling and planarization, we present a novel contact planarization process. In this process, the polymeric material that must fill in the vias or trenches is spin coated and baked on the topography wafer at an appropriate thickness. After the coating, voids are present inside the trenches and vias, as shown in figure 2. After the spin-coating process, a surface-modified pressure substrate is placed on top of the wafer. This assembly is then transported to the contact planarization tool. In this tool, the process chamber is evacuated and the polymer is heated using an infrared (IR) heat source. The IR heat source does not heat the silicon wafer or the surface-modified pressure substrate but heats only the polymer that needs planarization, thus saving process time and increasing throughput. As the chamber is evacuated and the polymer is heated, the viscosity of the

thermoplastic polymer drops, which allows "relaxation" of the polymer, which makes it more shapable, and provides the voids with the opportunity to escape from the film. After the polymer undergoes the relaxation process for a few minutes, pressure is applied to the pressure substrate from the center towards the edge, which forces all the excess polymer material on top of the topography wafer to fill the trenches and vias on the wafer. After this step, the wafer is removed from the tool and the surface-modified pressure substrate is easily separated from the topography wafer. The schematic of the contact planarization process is illustrated in figure 3.

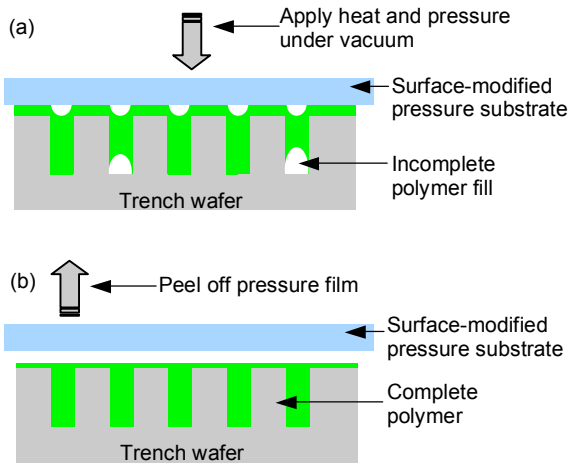

Figure 3. Schematic illustration of the contact planarization process

Operation Theory of Contact Planarization Tool

The contact planarization tool is a key element for this process. The object of contact planarization is to apply an evenly distributed force over a substrate surface for the purpose of planarization via a compressible fluid, i.e., air or nitrogen acting against a flexible membrane which in turn presses against the pressure substrate for planarizing the wafer.

The contact planarization tool contains three chambers filled with nitrogen or other gas in which the pressure is precisely controlled. There is an upper chamber, a middle chamber, and a lower chamber. The substrate to be planarized is contained in the middle volume. All these chambers have a flexible membrane as an interface between them.

In the first step to load the wafer, the lower chamber's pressure is reduced, which creates a space between the upper and lower membrane. The substrate can then be loaded onto the lower membrane. Then, all chambers are evacuated simultaneously while maintaining the pressure difference created in the first step between the lower and middle chambers. The lower volume has the highest vacuum applied, which keeps the substrate separated from the upper membrane. At this time, the wafer and the pressure substrate assembly are pre-heated to a temperature well above the glass transition temperature of the polymer using the IR light source. This pre-heating step allows the polymer to become more shapable, and the vacuum in the chamber allows for trapped air in the voids to escape from the trenches and vias. After the pre-heating step, the middle chamber is brought to the lower chamber's vacuum level. This equilibration does two things: it raises the lower membrane and bows the upper membrane. During this process the upper membrane comes into full contact with the substrate starting at the center and sweeping to the edge. This sweeping motion eliminates any potential trapped gases that can cause voids in the planarization material. Next the upper chamber is evacuated to match the lower and middle volume. The substrate is now in the press plane. Then pressure to the substrate is applied by inflating the upper and lower chambers either to ambient pressure or up to 100 psi by further pressurizing the two chambers. The middle chamber is still at the lowest possible vacuum. Then, while the pressure is being applied to the wafer and pressure substrate assembly, heat is also applied for a desired duration to achieve complete fill and planarization. Then pressure is released, and the stack is removed from the contact planarization tool. The stack consists of the pressure substrate in contact with the planarization material on top of the topography/device wafer. The last step is to remove the pressure substrate from the planarization material. Removal is performed by placing the stack, with the device side down, onto a chuck and securing with vacuum. Then a clamp assembly is used to lift the pressure substrate away from the planarization material. The modified surface of the pressure substrate allows for no stiction or other undesirable effects when the pressure substrate is removed from the planarization material. After this step, the trench- or via-filled device wafer is ready for downstream processes involving etch back of the planarization polymer through the rest of the process steps.

Results

The test structures shown in figure 1 were filled using the contact planarization process. In this process, the polymer material was coated and baked on the wafer and then processed through the contact planarization process. For the 400-µm test structure, the polymer was coated to have a 50-µm film thickness using the following process. The wafers were spin coated at 500 rpm for 10 s and then baked at 205ºC at 0.49-mm proximity for 2 min and then at 0.39-mm proximity

for 2 min, followed by a contact bake at 205ºC for 4 min. Then, the wafer, along with the planarizing substrate, was inserted in to the contact planarization tool where the assembly was preheated to 220ºC under vacuum for 3 min. Then at 220ºC pressure was applied for 2 min to the topography wafer through the planarizing substrate to fill and planarize the polymer on the topography wafer. After planarization, the wafer and the planarizing substrate were removed from the tool and cooled down. The planarizing substrate was then separated from the polymer film using the separator tool. Figure 4 shows SEM images of the two test structures that are completely filled following planarization.

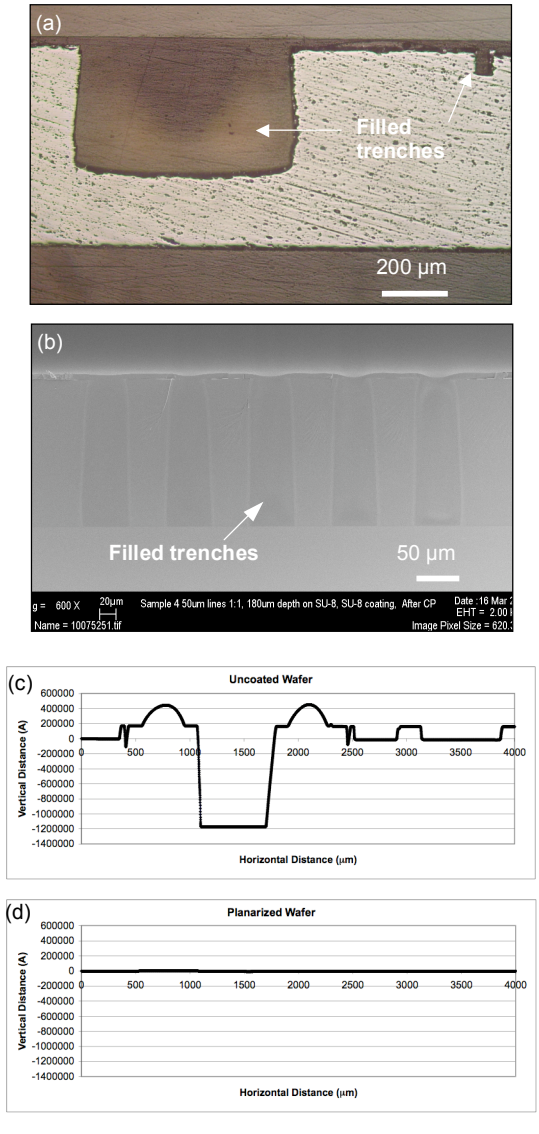

Figure 4. Images of filled trenches showing complete fill and planarization: (a) 400 µm deep trench (b) 180 µm deep trench with 50 µm width, (c) profile of wafer with 400 µm deep trench before spin coating, and (d) profile after planarization.

Figure 4 also shows profilometer scans of the topography wafer before coating and after planarization. The peak-to-valley topography before spin coating was ~ 430 µm, including the height of the glass frit. After planarization, the topography was less than 0.2 µm. The SEM image in figure 4(a) also shows the overburden on top of the glass frit. Overburden is defined the amount of material left on top of the highest region of the wafer surface. The overburden on top of the glass frit was ~ 5.3 µm.

The polymer was easily etched back using a plasma etching process. Using oxygen plasma under 60 mTorr, 400 W at 50 sccm flow rate, the etch rate for the polymer was ~ 0.55 µm/min. After the polymer etch-back process, the wafers can be used for downstream processes including photolithography and metallization.

Figure 5a shows the benchtop tool used for contact planarization. The tool is a single wafer process tool, with semiautomatic capability for planarizing the wafer. The tool uses manual loading and unloading processes for handling wafers. Figure 5b shows the wafer separator tool for separating the pressure substrate after planarization. This tool is also a semiautomatic tool with manual loading and unloading operations. An automated clamp assembly grabs the pressure substrate, and it is mechanically separated from the topography wafer. The surface modification on the pressure substrate assists in the separation process without causing stiction or adhesion issues to the polymeric planarization layer. After separating the pressure substrate from the device wafer, the pressure substrate can be reused multiple times for planarizing other device wafers.

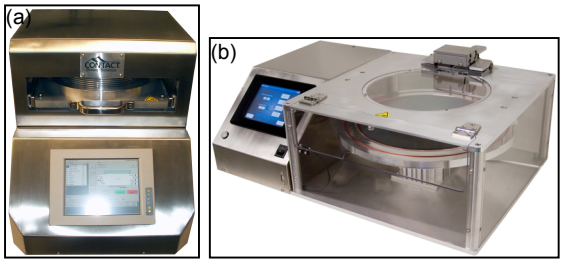

Figure 5. Photograph of (a) contact planarization tool and (b) separator tool.

Conclusions

In this paper, we have shown a novel method to fill deep vias and trenches with polymer. When heat and pressure are applied during the contact planarization process, the viscosity of the polymer drops due to the thermoplastic nature of polymer. Then, pressure is applied to the film using the pressure substrate, and

the polymer flows into the trenches while the voids are evacuated using vacuum. Finally, the pressure substrate is peeled off from the wafer using the separator tool resulting in completely planarized wafers with excellent via fill. The images show complete via filling with no voids. The oxygen plasma allows for etch back of the polymer to the wafer surface to enable further processing of the wafers.

Trench and via fill using a polymeric material has applications in polymer dielectric deposition TSV for 3-D integration and also in several other technology areas requiring planarizaiton of high-aspect-ratio or high-topography structures. The process demonstrated in this paper shows promise for using many thermoplastic polymers to fill structures for a variety of different applications.

References

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