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# **Extending Lithography with Advanced Materials**

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D.J. Guerrero, "Extending Lithography with Advanced Materials," *Proceedings of SPIE*, vol. 9051, paper no. 905114, 2014, doi: 10.1117/12.2047302.

Invited Paper

# **Extending Lithography with Advanced Materials**

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# ABSTRACT

Material evolution has been a key enabler of lithography nodes in the last 30 years. This paper explores the evolution of anti-reflective coatings and their transformation from materials that provide only reflection control to advanced multifunctional layers. It is expected that complementary processes that do not require a change in wavelength will continue to dominate the development of new devices and technology nodes. New device architecture, immersion lithography, negative-tone development, multiple patterning, and directed self-assembly have demonstrated the capabilities of extending lithography nodes beyond what anyone thought would be possible. New material advancements for future technology nodes are proposed.

Keywords: BARC evolution, semiconductor history, advanced materials

# 1. **DISCUSSION**

Material evolution and innovation has been a key driver for advancing technology nodes in the past 30 years. Brewer Science, Inc., has been a provider of commercially available anti-reflective coatings and ancillary coatings since 1981. Anti-reflective coatings are widely used in the photolithography process to minimize substrate reflection that occurs during imaging. Anti-reflective coatings evolved over time into multifunctional layers that together with advancements in resist chemistries have enabled technology nodes without changes imaging wavelength.

# 1.1 Evolution of anti-reflective coatings

An early publication on the use of an anti-reflective coating in a semiconductor substrate goes back to  $1970^1$ . This paper suggests the use of a dyed resist beneath a photoresist to mitigate the standing wave and uneven exposure that occurs when patterning a SiO<sub>2</sub> substrate. The paper described a theoretical solution to a problem; however, it lacked sufficient description on how to practically implement into a process. For example, there was no description of how to keep the dyed resist and top resist from intermixing or thickness or absorbance requirements. The proposed solution is illustrated in Figure 1.



Figure 1. Reflected wave effect (A) and antireflection solution (B) using dyed resist between substrate and resist. Source: Khoury and Patel, 1970<sup>1</sup>.

A later development described a similar solution to the anti-reflective wave effect<sup>2</sup>. As in the first paper, no description was provided in how to prevent the two resists layers from intermixing. None of the early papers provided a solution for removal of the anti-reflective film. In another attempt to solve the anti-

Advances in Patterning Materials and Processes XXXI, edited by Thomas I. Wallow, Christoph K. Hohle, Proc. of SPIE Vol. 9051, 905114 · © 2014 SPIE · CCC code: 0277-786X/14/\$18 · doi: 10.1117/12.2047302

reflective problem, the use of a very thin inorganic photoresist and a thick polymer layer was proposed<sup>3</sup>. This solution utilized a negative-tone photoresist composed from  $Ag_2Se/GeSe$  sensitive to 400-nm irradiation and a 2.5-µm film underneath to eliminate the standing wave effect. The thick film was removed using a plasma etch process. Patterning of a photoresist resulted in spaces where the anti-reflective film was exposed to the air interface. Eventually, the anti-reflective film had to be opened to the underlying substrate. In 1981, the solution for removal of the anti-reflective film that did not require a plasma etch step was proposed<sup>4</sup>. The proposed stack was very similar to the above-described dyed resist/resist stack. After exposing the first resist using a 400-nm light and development, a second exposure was carried out to open the dyed resist at DUV wavelengths. The top resist, being insensitive to DUV light, was not removed. Still, a practical commercial solution to this problem remained.

In 1981, Terry Brewer, founder of Brewer Science, published a paper in which he demonstrated an integrated solution to the anti-reflection control and film removal problem<sup>5</sup>. The key findings included the use of a high-absorbance dual-dye mixture, which allowed for thinner coatings, a developer-soluble film, which eliminated the use of plasma etch step, and good adhesion to substrate, which eliminated the need for adhesion promoters. A binary dye mixture was very important as one dye kept the other one in solution while both dyes contributed to the film absorbance. These findings made it possible to achieve critical dimension control (CD) in sub–1  $\mu$ m patterning. It also paved the way to a two-layer patterning system, bottom anti-reflective coating (BARC) plus resist.



Figure 2. Early experimental demonstration of elimination of standing wave using a BARC.

# 1.2 Technology driver: wavelengths vs. materials

From the early 1980s until today, there have been 4 changes in the wavelengths and substrate sizes used in the semiconductor industry. During the same period, CD was reduced from 1-µm to 40-nm dense structures using single-pass imaging. At the same time, Brewer Science and resist suppliers have advanced materials and photoresist performance to enable each technology node. BARCs became increasingly more complex, and ESCAP resists, topcoats, spin-on dielectrics, negative-tone imaging, and double and multiple patterning became available<sup>6</sup>. However, before this flurry of material evolution pushed technology forward, the most direct method for achieving the next technology node was to change the exposure wavelength. In a sense, physics was ahead of chemistry.

In a survey done by SEMATECH in 2001<sup>7</sup>, most companies concluded on which wavelength to use for each future technology node. The results are listed in table 1.

Technology	Preferred wavelength solution
node	
130 nm	KrF
90 nm	ArF
65 nm	F <sub>2</sub> (157 nm)
45 nm	EUV, EPL
32 nm	EUV

Table 1. Technology node and preferred imaging wavelength solution in 2001.

The  $F_2$  (157 nm) global initiative assembled one of the largest efforts observed in the industry at that time. Perhaps, not in economic terms but in the number of alliances brought together to make it a reality<sup>8</sup>. For example, there were 6 scanner manufacturers, 5 consortia, and 4 laser companies working on solutions for  $F_2$  patterning. In a short 3-year period, solutions to the technical challenges and economic payback for this technology did not come to realization. The industry felt that  $F_2$  technology would not result in sufficient technology nodes to warrant the investment and at the same time, ArF immersion was quickly gaining ground and became a replacement for  $F_2$  patterning. *The significance of this event is that changing wavelength stopped being the driving mode to achieve future nodes*. Since then, ArF immersion became the exposure wavelength and method for patterning used the longest. Extension of ArF immersion lithography until today has been enabled by materials innovation.

# 1.3 Imaging stack redefined

As ArF immersion lithography became dominant, the resist thicknesses began to decrease rapidly. An aspect ratio of 2:1 (height:width) is ideal for minimizing line collapse observed during the develop process. Smaller CDs required thinner resists. While resist thickness decreased, BARC thicknesses remained more or less constant, as the ideal thickness is roughly limited by material absorbance, refractive index, and wavelength of light used. The thickness of a BARC is adjusted to a quarter wave is defined by  $D = \lambda/4n$ , where n is the refractive index. The graph in Figure 3 shows the relationship between resist and BARC thickness trends over time.



Figure 3. Resist and BARC thickness trends over time.

The shrinking resist thickness created an unexpected problem during the pattern transfer process. As the resist thickness became closer to the BARC thickness, there was not sufficient resist remaining after the BARC etch to transfer the pattern into the substrate. To overcome this etch bias problem, two solutions were proposed. In one solution, the etch resistance property was transferred from the resist into an intermediate silicon-containing hardmask layer<sup>9</sup>. This layer also acted a BARC. Underneath the hardmask layer, a thick spin-on carbon (SOC) was used to planarize the substrate and effectively act as a pattern transfer layer. The etch rate differential between the hardmask and the SOC is very large, thus allowing for pattern transfer. The multilayer system is illustrated in Figure 4.

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Figure 4. Multilayer system for pattern transfer showing the hardmask/BARC layer plus SOC.

One of the critical parameters in multilayer systems is the chemical balance required throughout the whole stack. Changing the chemistry of the SOC can lead to completely different outcomes even while maintaining the same hardmask and resist<sup>10</sup>.

A second solution to the shrinking resist thickness problem was the development of developersoluble BARCs (DBARCs). Of interest to note is that the first BARCs developed by Brewer Science were in fact, developer soluble. As the industry adopted the use of BARCs, dry or plasma-etched BARCs became a more accepted technology for BARC removal. The reason being was that with shrinking line size, BARC CD could be controlled better using a dry-etch process than an aqueous developer. To overcome the limitations with undercutting or CD control in DBARCs, Brewer Science introduced the concept of photosensitive DBARC (PS DBARC) that allowed for better CD control and BARC removal only in the exposed areas<sup>11</sup>. Because the develop process is anisotropic, overdeveloped situations leading to line collapse are avoided. Figure 5 shows the difference profiles obtained between a DBARC and a PS DBARC.



Figure 5. Conventional DBARC (left) and PS DBARC (right). Conventional DBARC shows overdeveloped condition leading to line collapse.

### 1.4 Current lithography status

In 2013, ArF immersion lithography continues to be the workhorse of the industry. The 22-/20nm node was enabled with source mask optimization (SMO) and double patterning (DP). The 15-/14-nm node is being demonstrated using SMO plus double patterning (DP) and multiple patterning (MP) techniques. Early EUV is expected to support the 10-nm node, although the exact time currently is not known. Sub–10 nm nodes will mostly likely employ EUV (if available) or ArF immersion with directed self-assembly (DSA) techniques or self-aligned double patterning (SADP)<sup>12</sup>. Figure 6 shows the lithographic strategies used by the industry in the last decade<sup>13</sup>. Process and material innovation have made the extension of ArF immersion lithography possible for almost 10 years.



Figure 6. Lithography strategy in the last decade.

# 1.5 Future enabling materials

With the long-awaited advent of EUV lithography, new materials are being developed for 13.5-nm exposures. Because there is not mismatch of refractive indexes at this wavelength among most organic materials, reflection control is no longer an issue. However, reflection control is only one of many BARC functions. BARCs are also used for substrate planarization, adhesion promotion, chemical matching with resist, and protection from underlying contaminants and as a universal substrate on which to optimize resists platforms regardless of what is below the BARC. All of these properties will still be needed.

One of the current limitations in EUV lithography is the availability of photons reaching the photoresist, partly because of the output of the EUV sources but mainly because of the reflective optics used in the optical system. New underlayer materials are being designed to try to capture secondary electron generation that could lead to acid generation at the underlayer-resist interface<sup>14</sup>. It had been calculated that the thermalized electron probably distribution from the photon point of entry is about 10 nm<sup>15</sup>. More recently, it was calculated that the electron trajectory of a secondary electron is about 2-2.5 nm<sup>16</sup>, as shown in Figure 7. These distances are well within the critical interfacial region between an underlayer and resist where photochemical events can occur, and where the underlayer can have an influence on the resist performance.



Figure 9. Electron trajectory simulation for secondary electrons generated during EUV exposure.

We have shown that an improvement in resolution<sup>17,18</sup> and LER<sup>19</sup> can be achieved when using an underlayer beneath the resist in EUV lithography. We have also extended this concept to multilayer systems for EUV<sup>20</sup>. Although the mechanism on how the underlayers improve resist performance is not fully understood, it is believed that underlayer sensitization, chemical matching with resist, and diffusion control of chemical components between underlayer and resist are responsible for the improvements observed.

Another area of future research for new materials involves patterning without light by using DSA. Various processes have been described, and these fall within the two broad categories of either grapho-epitaxy or chemo-epitaxy processes<sup>21</sup>. In grapho-expitaxy, a resist pre-pattern is used to constrain the block copolymer (BCP) and alignment. In chemo-epitaxy, a chemical pattern (defined area with affinity to one of the blocks in the BCP) is used to induce alignment. Whichever method is used, most methods have common material needs: a pattern transfer scheme, anti-reflection control (for formation of pre-patterns), and a neutral layer and guide material.

In order to address the material needs and simplification of DSA processes, Brewer Science introduced a multifunctional layer that played the role of neutral layer, BARC, and hardmask needed for pattern transfer<sup>21</sup>. This hardmask neutral layer (HM-NL) reduces the need for three layers by combining their functions into a single layer. Figure 10 illustrates this process and compares it with the conventional approach.

Successful integration of a multifunctional HM-NL has been demonstrated in a contact hole shrink process<sup>22,23</sup>. Another solution targeted to address the poor etch differential bias between polystyrene-b-polymethyl methacrylate (PS-PMMA), the most common BCP under investigation, was recently proposed<sup>24</sup>. Typically, about 50% of the PS block is lost during the plasma etch process of PMMA. By increasing the etch resistance of PS, more etch budget is available for pattern transfer into the neutral layer or substrate.

The key to the early adoption of DSA processes will be simplification of steps and consolidation of materials having discrete functions into multifunctional layers. Each additional step or material introduces with it nuances associated with defect formation and control<sup>25</sup>. In the future, we envision multifunctional neutral layers with universal use for various types of BCPs as opposed to having neutral layers customized for a specific BCP.



Figure 10. Process flow using a hardmask neutral layer (HM NL) eliminates the neutral layer, BARC, and hardmask.

As IC designers continue to evolve device architecture from planar devices to silicon-on-insulator, to FinFET, and to the current tri-gate transistors, novel sacrificial materials are being developed to overcome problems encountered in the manufacturing process. For example, during the formation of the source and drain with high-energy implants, the latest FinFET devices can suffer from loss of Si lattice crystallinity. This is caused by the high-energy ions hitting the Si fins and amorphizing a few nanometers from the surface<sup>26</sup>. Amorphization changes the amount of de-channeling and defect formation. A method to overcome this problem is to raise the implantation temperature. Increasing the temperature enhances dynamic annealing and increases the dose required for Si amorphous layer formation. Figure 11 shows the fin morphology difference observed between room temperature and elevated temperature implant.



Figure 11. Fin morphology after implantation at ambient (left) and high temperature (right). High crystallinity is obtained when using high-temperature implantation. Source: ref. 26.

Brewer Science developed SOC layers able to withstand temperatures up to 600°C needed for masking areas that need to be protected during the hot implantation process. Figure 12 illustrates how a high-temperature SOC is used during the implantation process. Figure 13 shows the thermogravimetric analysis of a high-temperature SOC (HT SOC) layer demonstrating stability during heating up to 600°C.



Figure 12. Scheme showing the use of high-temperature SOC during fin implantation.



Figure 13. Thermogravimetry analysis of high temperature SOC layer (HT SOC) showing the thermal stability needed for high-temperature implantation processes.

New device architectures being proposed to evolve from FinFET to more advanced devices includes placement of the gate completely around the channel. Figure 14 illustrates the evolution of device architecture for each technology node<sup>27</sup>. Gate all around approaches will create devices stacked in either vertical or horizontal positions<sup>28</sup>. New materials will be needed to create these structures. Some groups have already proposed the use of DSA techniques to create Si cylinders or pillars needed for achieving these device geometries<sup>29</sup>. An SEM photo of these nanopillars is shown in Figure 15.



Figure 14. Evolution of device architecture for each technology node.



Figure 15. Silicon nanowires 16 nm wide and 200 nm tall made using DSA techniques.

Although most do not associate change in substrate size as having significant impact in material design, the expected move to 450-mm wafers should not be overlooked from a material point of view. It is understood that the next substrate size provides economic benefits rather than a technical advantage. Because of the larger area, twice as many dies for memory devices will be printed on a single wafer relative to the current 300-mm wafers<sup>30</sup>. Our experience from the 200- to 300-mm transition showed that as spin bowls and bake ovens inside coating tracks became larger, the flow and air dynamics inside the chambers changed enough to have an effect on coating performance. For example, solvent and small molecule outgassing that can occur during the bake process that was at acceptable levels with the smaller substrates reached unacceptable levels inside 300-mm chambers. To address uniformity across a wafer while spinning at low rpm, planarization over large-area topography, and exhaust and air flow during bake and spin, we expect it will be likely that existing materials will require reformulation and/or rheological properties of polymers will require adjustment. More viscosities of the same material will also have to be available as the spinning range of a 450-mm wafer is at most 400–500 rpm. Adjustment of wide thickness targets via rpm adjustments of a single viscosity material will not be possible.

## 2. CONCLUSIONS

In the last 30 years Brewer Science and the resist community have been key enablers of technology for the industry by providing early solutions to lithographic challenges. New device architecture, immersion lithography, negative-tone development, multiple patterning, and DSA have demonstrated the capabilities of extending lithography nodes, particularly ArF immersion, solely by utilizing innovative processes and materials. Brewer Science will continue to support prior and future nodes by evolving materials and innovating new concepts for EUV, DSA, new device architectures, and multiple-patterning technologies.

#### **3. ACKNOWLEDGEMENTS**

The author would like to acknowledge the useful discussions and information provided by Plamen Tzviatkov from FFEM, Ralph Dammel from AZ-EM, Xavier Buch from JSR, Jim Cameron from Dow Electronic Materials, and Monique Ercken and Mieke Goethals from imec.

# 4. REFERENCES

- Khoury, H. A.; Patel, K. V. "Anti-interference phenomena coating," *IBM Technical Bull.*, 13 (1), June 1970.
- [2] DiPiazza, J. J. "Nonreflecting Photoresist Process," US Pat. 4,102,683, July 1978.
- [3] Tai, K. L.; Sinclair, W. R.; Vadimsky, R. G.; Moran, J. M. "Bilevel high resolution pholithographic

technique for use with wafers with stepped and/or reflecting surfaces," J. Vac. Sci. Technol., 16 (6), (1979).

- [4] O'Toole, M. M.; Liu, E. D.; Chang, M. S. "Linewidth control in projection lithography using a multilayer resist process," *Electron Devices, IEEE Trans.*, 28 (11), November 1981.
- [5] Brewer, T.; Arnold, J. W. "The reduction of standing-wave effect in positive photoresist," SPSE 33<sup>rd</sup> Annual Conference, results published in J. Appl. Photographic Eng., 7 (6), 184-187, December 1981.
- [6] Key enablers were: ESCAP resist by Dow, top coats by JSR, spin-on dielectrics for high aspect ratio trench filling by AZ-EM, and negative tone development by FFEM. Most resist suppliers contributed to double resist patterning strategies.
- [7] Sematech 5<sup>th</sup> NGL workshop, Pasadena, CA, August 28-30, (2001).
- [8] In terms of cost, EUV lithography is probably the most expensive lithographic technology to date. http://www.lithoguru.com/scientist/essays/EUV\_SST.html
- [9] Meador, J. M.; Holmes, D.; Nagatkina, M.; Puligadda, R.; Gum, D.; Bennett, R.; Sun, S.; Enomoto, T. "New Materials for 193-nm Trilayer Imaging," *Proceedings of SPIE: Advances in Resist Technology* and Processing XXI, vol. 5376, pp. 1138-1148, (2004).
- [10] Guerrero, D. J.; Krishnamurthy, V.; Sullivan, D. M. "BARC surface property matching for negativetone development of a conventional positive-tone photoresist," *Proceedings of SPIE*, vol. 7972, pp. 79720Q-1 - 79720Q-7, (2011).
- [11] Guerrero, D. J.; Trudgeon, T. "A New Generation of Bottom Anti-Reflective Coatings (BARCs): Photodefinable BARCs," *Proceedings of SPIE: Advances in Resist Technology and Processing XX*, vol. 5040, pp. 1386-1395, (2003).
- [12] Oyama, K. "Robust complementary technique with multiple-patterning for sub-10nm node device", *Proceedings of SPIE: Advances in Patterning Materials and Processing XXX1*, vol. 9051-30, in press, (2014).
- [13] Umatate, T. Lithography Workshop, November 2010.
- [14] Guerrero, D. J.; Beaman, C.; Sakamoto, R.; Endo, T.; Ho, B-C. "Organic Underlayers for EUV lithography," J. Photopolym. Sci. Techn., vol. 21 (3), 451-455, (2008).
- [15] Kozawa, T.; Tagawa, S.; Cao, H. B.; Deng, H.; Leeson, M. J. "Acid distribution in chemically amplified extreme ultraviolet resist," J. Vac. Sci. Technol. B, vol. 25, 2481-2485, (2007).
- [16] Denbeaux, G.; Torok, J.; Del Re, R.; Herbol, H.; Das, S.; Bocharova, I.; Paolucci, A.; Ocola, L. E.; Ventrice, C.; Lifshin, E.; Brainard, R. "Measurement of the role of secondary electrons in EUV resist and exposures," EUV Workshop, Maui, 2013. https://www.euvlitho.com/index.php?\_a=viewDoc&docId=41
- [17] Xu, H.; Blackwell, J. M.; Younkin, T. R.; Min, K. "Underlayer designs to enhance the performance of EUV resists," *Proceedings of SPIE*, vol. 7273, pp. 7273J-17273J-11, (2009).
- [18] Guerrero, D. J. Xu, H.; Beaman, C.; Sakamoto, R.; Endo, T.; Ho, B-C. "Effects of underlayers on EUV lithography," 2008 International EUVL Symposium [SEMATECH], Lake Tahoe, CA, Sept. 28-Oct. 1, (2008).

- [19] Goethals, A. M.: Niroomand, A.; Ban, K.; Hosokawa, K.; Roey, F. V.; Pollentier, I.; Jehoul, C.; Heuvel, D.; Ronse, K. "EUV resist performance, progress and process improvements at imec," EUVL Symposium, Kobe, October 2010.
- [20] Ouattara, T.; Washburn, C.; Collin, A.; Krishnamurthy, V.; Guerrero, D. J.; Weigand, M. "EUV assist layers for use in multilayer processes," *Proceedings of SPIE*, vol. 8322, pp. 83222E-1 – 83222E-7, (2012).
- [21] Rathsack, B., Somervell, M.; Hooge, J.; Muramatsu, M.; Tanouchi, K.; Kitano, T.; Nishimura, E.; Yatsuda, K.; Nagahara, S.; Hiroyuki, I.; Akai, K.; Hayakawa, T., "Pattern scaling with directed self assembly through lithography and etch process integration," *Proceedings of SPIE*, vol. 8323, 2012, 83230B, (2012).
- [22] Guerrero, D. J.; Hockey, M. A.; Wang, Y.; Calderas, E. "Multifunctional hardmask neutral layer for directed self-assembly (DSA) patterning," *Proceedings of SPIE*, vol. 8680, 86801P, (2013).
- [23] Romo-Negreira, A.; Younkin, T. R.; Gronheid, R.; Demuynck, S.; Vandenbroeck N.; Seo, T.; Guerrero, D. J.; Parnell, D.; Muramatsu, M.; Shinichiro, K.; Takashi, Y.; Nafus, K.; Somervell, M. H. "Evaluation of integration schemes for contact-hole grapho-epitaxy DSA: A study of substrate and template affinity control," *Proceedings of SPIE: Advances in Patterning Materials and Processing XXX1*, vol. 9049-56, in press, (2014).
- [24] Hockey, M. A.; Kui, X.; Wang, Y.; Guerrero, D. J.; Calderas, E. "Streamlined etch integration with a unique hardmask neutral layer (HM-NL) for self-assembled block copolymers (BCPs)," *Proceedings of SPIE*, vol. 9049-83, in press, (2014).
- [25] Gronheid, R.; Vandenbroeck, N.; Sayan, S.; Romo-Negreira, A.; Somervell, M. H. "Process optimization of template DSA flows," *Proceedings of SPIE*, vol. 9051-17, in press, (2014).
- [26] Wood, B.; Colombeau, B.; Sun, S; Waite, A.; Chen, H.; Jin, M.; Chan, O.; Khaja, F.; Thanigaivelan, T.; Pradhan, N.; Gossmann, H.-J.; Sharma, S.; Chavva, V.; Cai, M-P.; Okazaki, M.; Munnangi, S.; Ni, C-N.; Suen, W.; Chang, C-P.; Mayur, N.; Variam, N.; Brand, A. "Fin Doping by Hot Implant for 14nm FinFET Technology and Beyond," Abstract 2237, 224<sup>th</sup> ECS Meeting, (2013).
- [27] Courtesy of Naoto Horiguchi, Logic Program at imec.
- [28] Bangsaruntip, S.; Cohen, G. M.; Brink, M.; Tsai, H.; Engelmann, S. U.; Newbury, J. S.; Gignac, L. M.; Breslin, C. M.; Klaus, D. P.; Guillorn, M. A. "30nm pitch compatible, stepwise hydrogen anneal for LER reduction on silicon nanowires," *Proceedings of SPIE*, vol. 9054-10, in press, (2014).
- [29] Goshai, T.; Senthamaraikannan, R.; Shaw, T.; Holmes, J. D.; Morris, M. A. "An insitu hardmask block copolymer approach for the fabrication of ordered, large scale, horizontal aligned, Si nanowire arrays on Si substrate," *Proceedings of SPIE*, vol. 9051-18, 2014, in press. Also in *Nanoscale*, vol. 4, 7743, (2012).
- [30] Higashiki, T. Panel Discussion, EUV Workshop, Maui, 2013. https://www.euvlitho.com/index.php?\_a=viewDoc&docId=41