Developer-soluble Gap fill materials for patterning metal trenches in Via-first Dual Damascene process

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ABSTRACT

This paper discusses a novel approach of using a developer-soluble gap fill material[1], wherein the gap fill material is coated in a layer thick enough to planarize all the topography and is then recessed using a standard 0.26N TMAH developer. The material recess process takes place in the same coater track where it is coated and therefore simplifies the process and increases wafer throughput. Performance and properties of two types of developer-soluble gap fill materials (EXP03049 and NCA2528) based on two different polymer platforms will be discussed in detail.

Keywords: Gap fill material, Via-first Dual Damascene (DD) process, iso-dense fill bias, Developer

1. INTRODUCTION

The need for constant reduction in critical dimensions (CD) of integrated circuits (ICs) to make them faster has been the driving force for next-generation lithography. Copper is slowly replacing aluminum as the interconnect material in advanced ICs manufactured using either single inlay or DD processes. The transition from aluminum as a conducting metal to copper has been difficult one with many material and process challenges.

The conventional method of patterning trenches in a via-first DD process involves filling the vias with a dry-etch organic bottom anti-reflective coating (BARC)[2], applying the photoresist and then performing trench lithography. Typically a semiconductor substrate will have dense/isolated via arrays and large open areas where there are no via holes. A conventional organic via fill BARC does a poor job of planarizing the substrate. A large fill bias between the isolated and dense via arrays is usually observed when such a process is used (Figure 1), the bias can be as high as 100 to 150nm depending on via size and density. This huge fill bias creates problems during trench lithography by narrowing down the process latitude and causing overetching in the dense via arrays during final trench etch, which eventually creates different trench depths across the via arrays. Another approach, currently being used is to apply a thick layer of material, which does not need to have anti-reflective properties but can fill via holes and planarize the topography. These materials are often referred as a gap fill materials. Modified i-line photoresists have been commonly used as gap fill materials to planarize topography. Gap fill materials are applied to the substrate and then etched back by using either a reactive ion etch (RIE) process or chemical mechanical polishing (CMP)[3]. The substrate is then coated with a conventional KrF or ArF BARC to provide reflectivity control. Coating a thick material to planarize topography reduces the isolated-dense via fill bias, which results into wider lithography and etch latitude. The process mentioned above requires wafers, which are coated with the gap fill material, to be transferred to the Etch/CMP tool for the etch-back step and brought back to the photo bay for BARC coating and trench lithography. This transfer process is cumbersome, reduces the wafer throughput and could generate particles during the multiple wafer handling steps involved. Furthermore using the RIE process to do a recess to the substrate could damage alignment marks on the wafer. A bilayer process is used by some IC makers, on back-end layers as an alternative to the gap fill, dry etch-back process. The silicon-containing photoresist used in the bilayer process has its own problems, for instance, line edge roughness (LER) and narrow process latitude, to name a few. Other alternatives have been proposed to move away from the dry RIE and bilayer process. One of them involves using a conventional EBR solvent[4] and other uses a developer-soluble gap fill material to do a recess to the substrate. The latter will be discussed in detail in this paper, which outlines the different integration schemes.

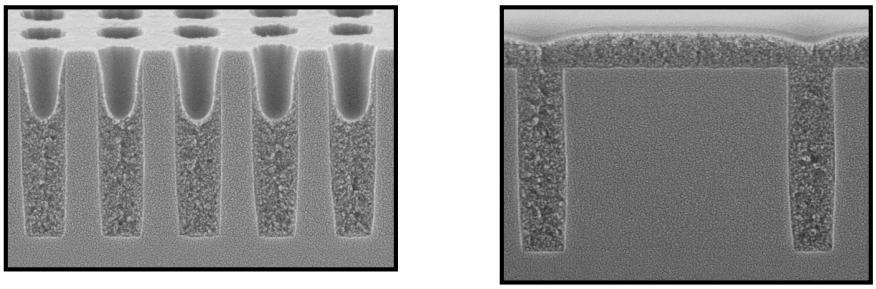


Figure 1. Iso-dense fill bias seen with conventional full via fill materials.

Developer soluble BARCs have been traditionally used for lift off and more recently are being evaluated for front-end processes such as implant layers. These materials simplify processing because they do not need a BARC open-etch step normally required by conventional dry-etch BARCs and thereby improve the etch budget. Developer-soluble materials, unlike dry-etch materials are more sensitive to bake temperature and their performance could be adjusted during the bake or the develop process. Figure 2 shows a schematic process flow for a developer-soluble gap fill material to planarize topography (using two schemes) in a via-first DD sequence.

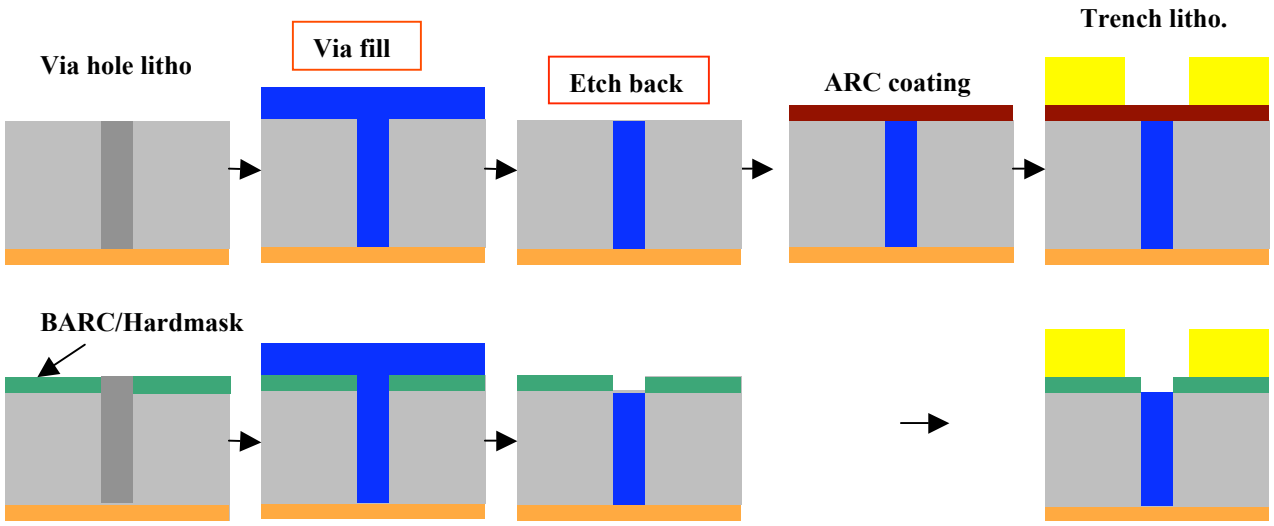


Figure 2. Schematic for patterning metal trenches using gap-fill material (via-first DD process) with a spin-on organic BARC and an inorganic BARC/hardmask approach.

2. EXPERIMENTAL

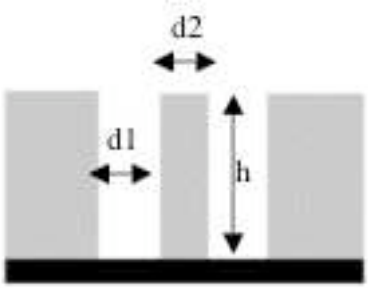
All the gap fill materials were formulated to achieve a thickness of about 300nm on a flat silicon wafer. The substrates used for via fill testing were obtained from International Sematech (ISMT) and IMEC and consisted of isolated and nested via arrays across the wafer. The via dimensions were 250nm x 700nm on ISMT wafers and 220nm x 100nm on IMEC wafers. The wafers and in some cases wafer chips used for via fill testing were coated using a TEL Mark8, DNS clean track and CEE 100 bench top spinners respectively. Measurements and cross-sections were done using a LEO 1560 SEM. Wafers with different dielectrics and organic BARCs were blanket etched on a Nippon Scientific Company etcher in Japan.

3. RESULTS AND DISCUSSION

Two formulations based on two different polymer platforms were characterized. These developer-soluble gap fill materials are versatile, and can be used with different schemes or process flows. The three schemes we propose are:

1. Doing a recess using a developer and stopping at the substrate or top of the via
2. Doing a recess inside the via to get different degrees of partial fill
3. Doing a partial recess wherein the material recess is stopped at a 1st or 2nd reflectivity minimum of the material.

In all the options mentioned above, the gap fill material is coated thick enough to planarize all the topography present on the wafer. Fill bias between isolated and nested vias is dependent on the thickness of the film, via size, via pitch, and density. One of the mathematical equations predicting theoretical iso-dense fill bias is shown in Figure 3. A smaller area ratio (A), smaller via depth (h) and a higher solid content (S) coresponds to a smaller fill bias.



d1= hole width
d2= Space width
h= Hole depth
S= Solid content (10%=0.1)
A= Area ratio

$$A = \frac{\{(d1/2)^2 * \pi\}}{\{d1+d2\}^2}$$

If 1:1 spacing, d1=d2, $A = 16/\pi$

Iso-dense fill bias = A*(1-S) *h

Figure 3. Equation predicting theoretical isolated-dense via fill bias.

The film is then baked at a temperature between 160C-220C for 60s. The bake temperature controls the develop rate of the film in the developer, specifically, baking the film at a higher temperature reduces the develop rate and vice versa. A standard 0.26N developer is then puddled on the film for 30-60s depending on the type of scheme used. The develop time also dictates the amount of film that would be left over after the wet recess. A partial fill or recess inside the via can be achieved by either longer develop times or lower bake temperatures. A conventional spin organic or a PECVD-deposited inorganic BARC (which also acts as a hardmask) provides reflectivity control during the trench lithography process. The first two schemes are relatively easy and robust, while the third scheme is difficult and requires tight control during the develop step because of the need to stop at a certain film thickness. The film also requires an extra bake step (not required for schemes one and two) for removing any residual developer present in the film to prevent poisoning of the photoresist. The photoresist is then directly applied on the recessed film, followed by trench lithography. Using this scheme requires that the gap fill material have absorbance at the wavelength of interest because the fill material will act as a BARC during lithography, Table 1 shows the n and k values of the materials evaluated. A dye can be added to these formulations to provide appropriate extinction coefficients for adequate reflectivity control at the wavelength of interest. The dye not only gives the required n and k values but also controls the develop rate. A dye having a high amount of phenol or carboxylic acid moieties will be more base soluble and the amount of dye put in the formulation can be varied to adjust the develop rates. Figure 4 compares the process flows for a conventional RIE scheme and a process using a developer-soluble gap fill material.

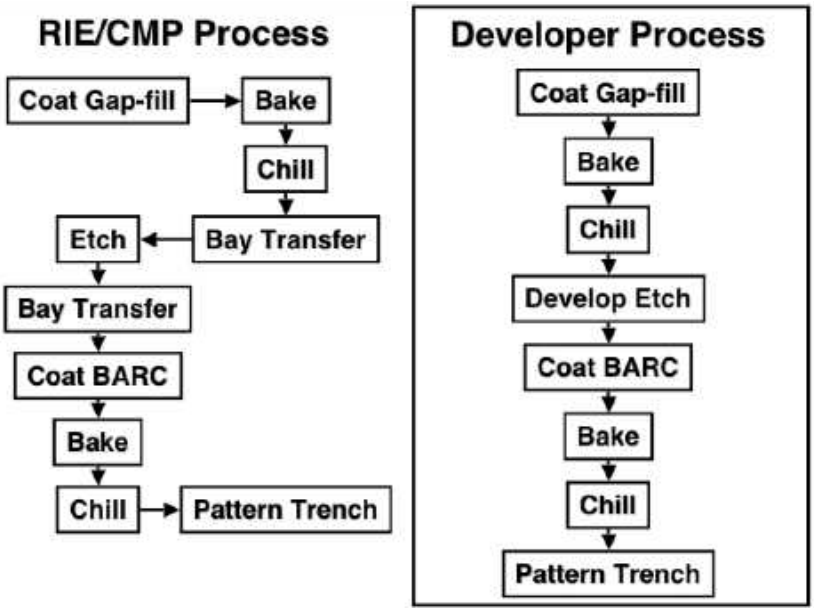


Figure 4. Comparison between conventional RIE/CMP process and developer recess process. □

Fencing or crowning defects are commonly seen with conventional full via fill materials. The main reason for these types of defects is the bias between the etch rates of the fill material and the inter-level dielectric (ILD). If the BARC fill material etches slower than the ILD in the trench etch gas recipe, a crown or a fence is created on the top of the trench after the etch process. This fence or crown is difficult to remove and creates problems during copper seed layer deposition and plating. Doing a recess inside the via (scheme 2) approximately equal to the height of the trench, to achieve partial fill, can prevent formation of fences or crowns. NCA2528 and EXP03049 show good selectivity to oxide and other low-κ dielectric materials in a CF_4 etch gas recipe (Figure 5).

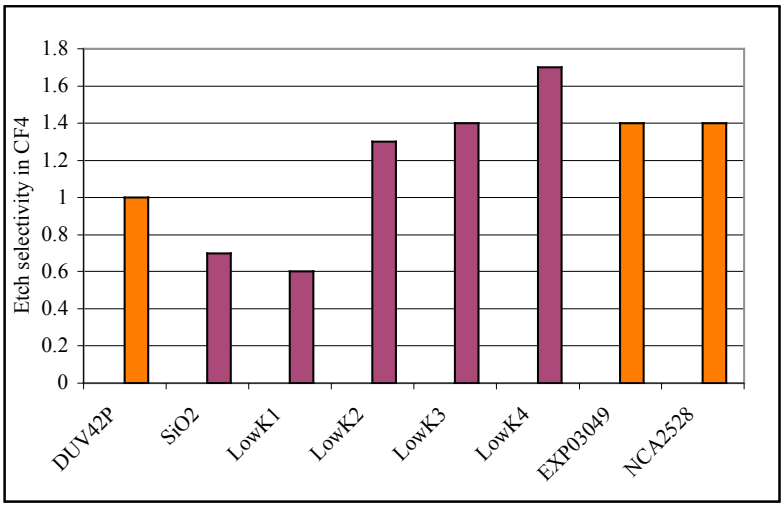


Figure 5. Etch selectivity of developer-soluble gap fill materials to commonly used ILDs.

Dissolution rate is the single most important property of these fill materials. The films are composed of thermoset polymers, which upon hot plate cure form a crosslinked structure and cannot be stripped in common EBR solvents. Considering the process takes place in a controlled clean room environment (constant relative humidity and temperature), dissolution rate of a film in a developer is a function of the bake temperature and bake time. Bake temperature has the biggest effect on dissolution rate of the film (Figure 6).

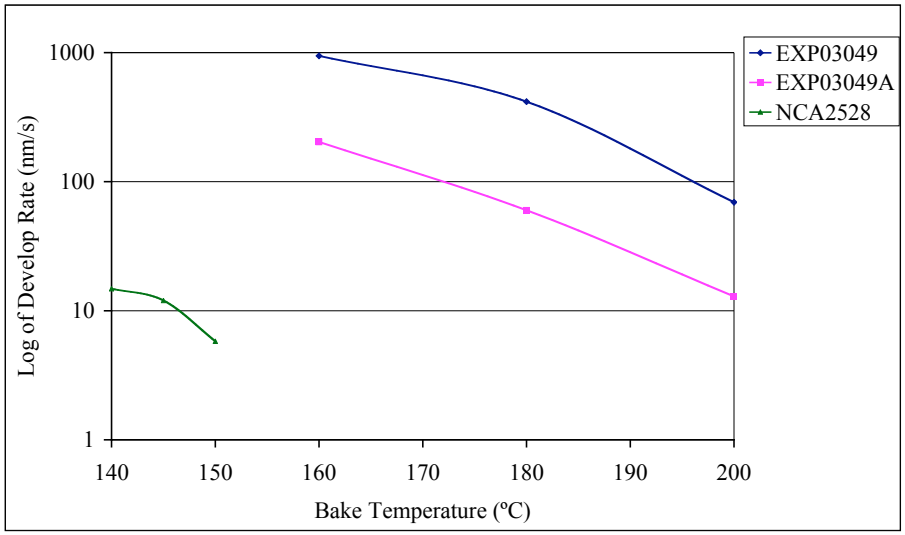


Figure 6. Bulk develop rate of gap fill materials as a function of temperature.

Different degrees of fill in the via hole can be obtained either by changing the bake temperature or the developer recess times (figures 8-11). Dissolution rate decreases as the bake temperature increases due to tighter crosslinking of the polymer film. The bulk develop rate of the film is different from the develop rate of the film in the via hole, and therefore material inside the via develops at a slower rate than the material on the top of the via. Two possible reasons for this phenomenon would be higher polymer crosslink density inside the via hole due to more heat transferred from the surrounding ILD (compared to heat transferred to the material in the bulk) because of more surface area. Also, the developer is more efficient in the open areas than inside the via hole. The small size of the hole limits fresh developer from coming in constant contact with the fill material, and the dissolution rate drops significantly.

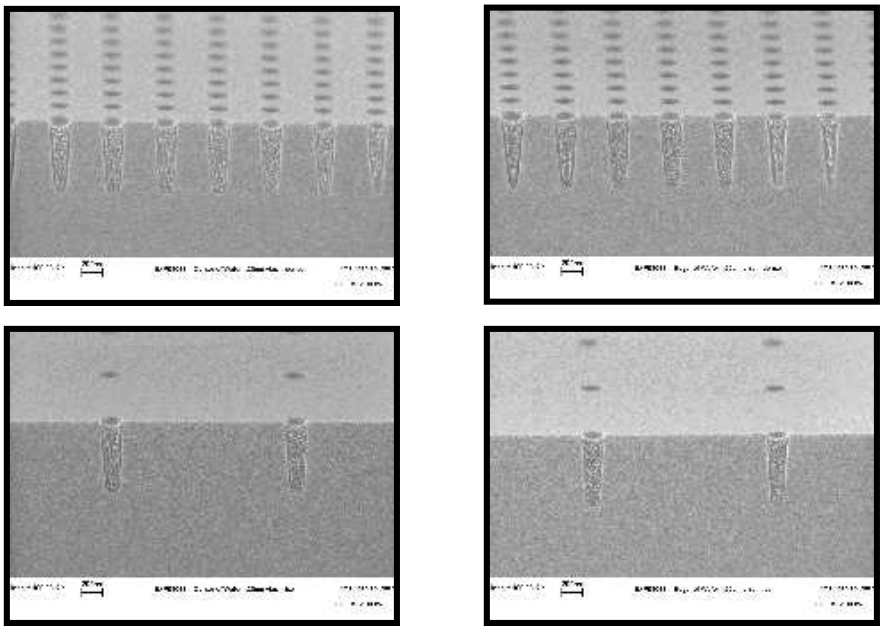
3.1 Gap Fill Product Performance

Two gap fill formulations, EXP03049 and NCA2528, were used to perform testing and characterization work. All the samples tested were formulated to achieve a thickness of around 300nm on flat silicon wafers at a spin speed of 1500rpm. EXP03049 can be used as gap fill materials as well as BARCs at 193nm and 248nm, while NCA2528 is strictly a gap fill material at 248nm (no absorbance) but can act as a BARC layer at 193nm.

	n	k
EXP03049		
193nm	1.45	0.43
248nm	1.8	0.42
633nm	1.61	0
NCA2528		
193nm	1.56	0.51
248nm	1.62	0.08
633nm	1.54	0

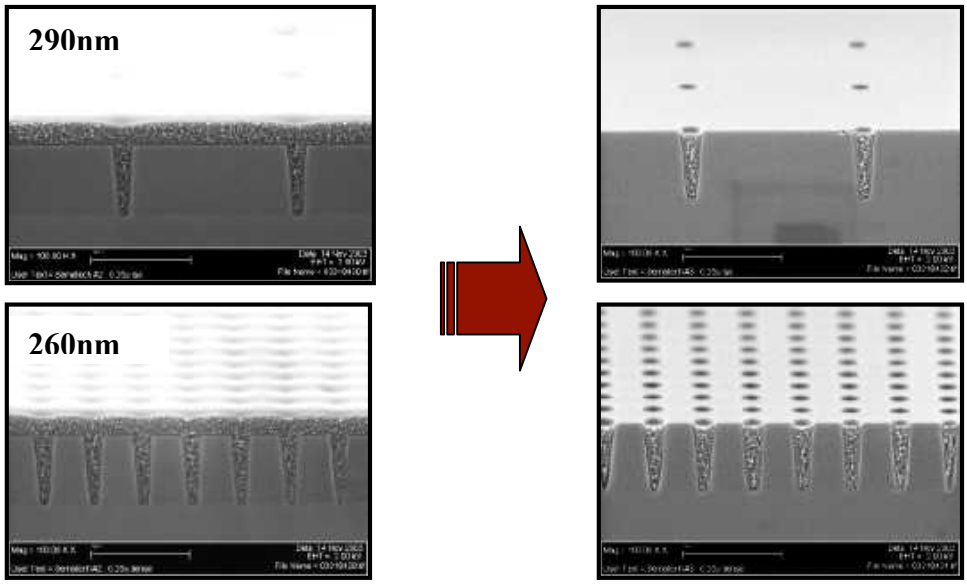
Table 1. Optical properties of via fill materials.

Fill bias between isolated and dense via arrays has been the primary metric to evaluate gap fill formulations after the developer recess process, but across-wafer uniformity after developer recess is also important in order to ensure good CD control during trench lithography. EXP03049 and NCA2528 show excellent across-wafer uniformity on an 8-inch via wafer done using a single puddle develop process. No center-to-edge uniformity issues were observed.



Center Edge

Figure 7. Across-wafer uniformity of developer-soluble gap fill material.



Before developer recess After developer recess (60s single puddle)

Figure 8. Developer recess up to the via tops with EXP03049 (180C/60s bake, 60s single puddle).

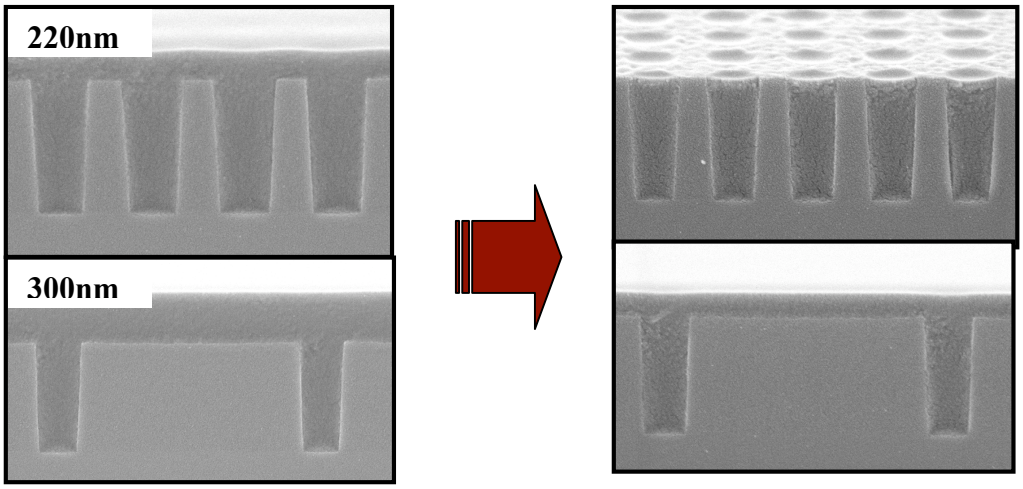
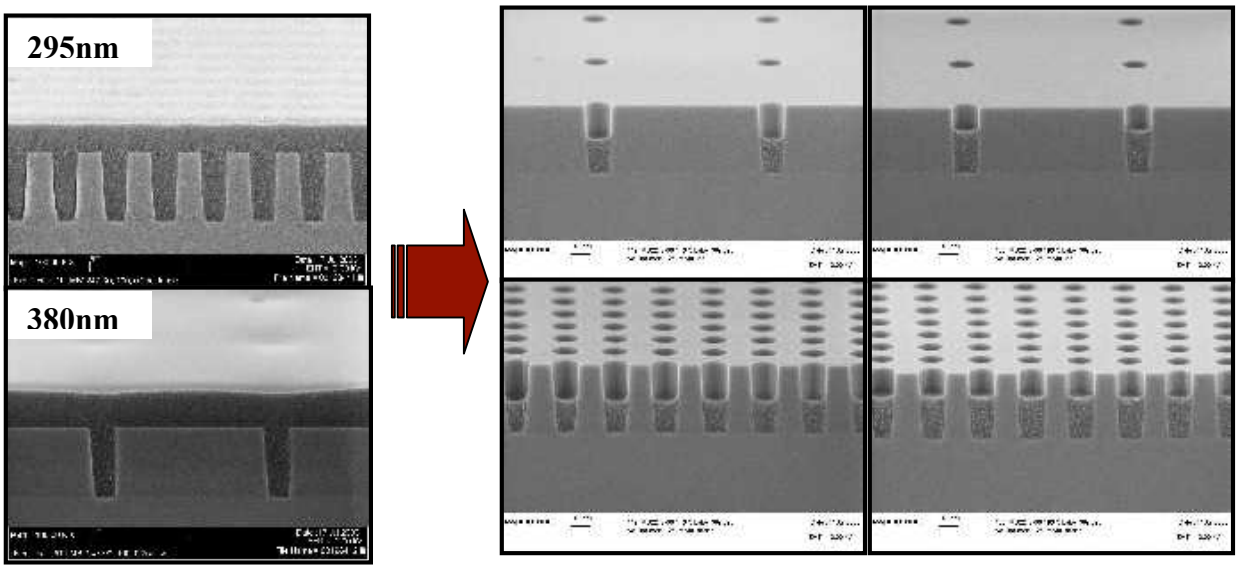


Figure 9. Developer recess up to the via tops using NCA2528 (160C/60s, 60s single puddle).



140C/60s, 30s develop 160C/60s, 30s develop

Figure 10. Partial via fill by changing bake temperature for EXP03049.

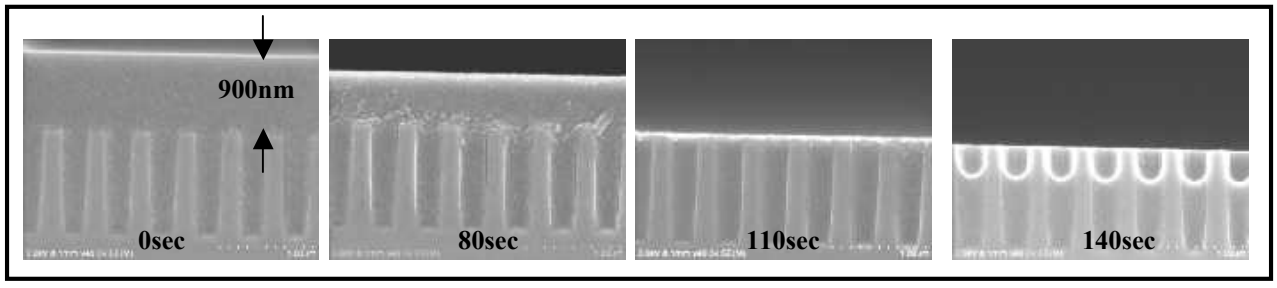


Figure 11. Different degrees of via fill using different developer recess times with NCA2528.

4. CONCLUSIONS

Performance of two developer-soluble via fill materials, EXP03049 and NCA2528, was discussed in this paper. Developer-soluble gap fill materials provide an excellent alternative to existing dry RIE and CMP processes used to achieve a planar surface required for resist coat and trench lithography. The gap fill material coat/bake and developer recess takes place in the same coater track, which eliminates the need to transfer wafers to RIE or CMP bays. This increases wafer throughput, reduces wafer handling multiple times, and can reduce generation of particles. These materials show excellent planarization properties and reduce the isolated-dense via fill bias.

EXP03049 and NCA2528 show good etch selectivity to commonly used ILDs. Via fill properties of these developer-soluble materials can be adjusted, to get full or partial fill, by changing the bake temperature or the developer recess time. Good etch selectivity to ILD and flexibility to get different degrees of via fill can resolve integration issues like fence or crown formation after final trench etch.

5. ACKNOWLEDGEMENTS

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