# Advanced developer-soluble gap-fill materials and applications

Runhui Huang, Dan Sullivan, Anwei Qin, Shannon Brown
Brewer Science, Inc., 2401 Brewer Dr., Rolla, MO, USA, 65401

## ABSTRACT

For the via-first dual damascene process, a planarizing anti-reflective material and gap-fill material are typically used to ensure a lithography process produces the best profiles and critical dimension (CD) control and integration small feature size structure. Traditional gap-fill materials is usually coated in a thick layer, followed by plasma etching to remove extra gap-fill material above the substrate surface. We have developed a unique developer-soluble gap-fill material, BSI.G05013, which can be etched back in standard photoresist developer, instead of plasma beam. By careful design of both the polymer and formulation, our developer-soluble gap-fill materials fill vias and trenches on different substrates without void formation. Also, these gap-fill materials do not exhibit swelling or peeling problems during the developer etch-back process. Dissolution rate is adjustable by customizing the material with regard to the chemical structure of the polymer and the formulation composition. This new generation developer-soluble gap-fill material has broad process windrow on bake temperature and develop time. The local bias between dense and isolated via areas, the global bias from wafer center to edge are significantly reduced after develop back due to the dissolution rate difference between the bulk material and the material inside of the vias. Material is spin bowl compatible, no precipitation in rinsing solvents. It is stable in storage condition for a long period. Both dry plasma clean and wet developer clean can be used to remove the residual gap-fill material after process. The new generation develop-soluble gap-fill material, BSI.G05013 is robust, the process is economically favorable, which is a convenient solution to achieve planarizing surface.

Key words: dual damascene, gap fill, via fill, developer soluble, planarizing

## 1. INTRODUCTION

In the integrated circuit (IC) industry, the transistors become faster, smaller, cheaper, and more efficient as electronic devices become more portable and accessible. As the feature sizes of transistors continuously shrink and the density of transistors on chips further increases, the electrical resistance and parasitic capacitance with back-end-of-line aluminum interconnections have grown into major factors that limit the circuit speed of high-performance ICs [1]. To overcome these problems, the copper dual damascene process for metal interconnection and low-k materials for interlayer dielectrics has been integrated into IC device fabrication. In this process, deep vias are formed first; trench structures must be created over topography that is resulting from the previous via-etch step. Dual damascene processing presents a tremendous challenge to lithographers for the resist coating, exposure, and development processes [2].

The thickness bias between dense and isolated via areas narrows down the resist process window, and causes trench critical dimension (CD) out of control. Traditional lithography processes utilizing photoresists and conventional organic anti-reflective coatings cannot meet the planarizing requirement of small feature size integration structure. A gap-fill material is needed in dual damascene process to fill the high aspect ratio vias without void and reduce dense and isolated bias significantly. A good planarize surface ensures that the lithography process has results in the best profiles and critical dimension control [3,4]. This gap-fill material not only reduces the surface topography, but also prevents over-etching the underlying metal or transistor structures at the base of the vias while the trench is being etched [5]. The technology of planarizing surface becomes more important for advanced lithography, and other applications, such as MEMS. Gap- fill material has been used widely on filling vias, trenches, and also other different kind of gaps.

The traditional gap-fill material is applied on a high aspect ratio substrate as a thick layer in order to cover topography and achieve low thickness bias between dense and isolated feature areas. This step is often followed by plasma etching to remove extra gap-fill material that is above the substrate surface, in the result of leaving only filled vias. The plasma etch step includes bay transfer, etch, clean, and bay transfer again [6], which is expensive on tool and process time, and also is a potential source of defect generation, such as particles, fence and crown. Instead of using a plasma etch process, developer-soluble gap-fill materials can be etched back to the substrate surface by using a standard photoresist

developer, 0.26N tetramethylammonium hydroxide water solution, which provides the advantages of simplifying the process, decreasing the cost, reducing defects, and eliminating plasma damage. The developer-soluble gap-fill materials can be removed by ether plasma ashing or developer washing.

## 2. EXPERIMENTS

### 2.1. Synthesis and formulation

Polymer was synthesized in lab scale and pilot scale reactors in Brewer Science. Reaction temperature, time, and catalyst loading were controlled to obtain the desired polymer properties. Formulations were prepared by blending appropriate amounts of polymer, additives and solvents. The finial solutions were filtered through 0.1-0.02μm filter.

### 2.2. Characterization

The wafers were coated using a Cee 100CB combination spinner/hotplate under spin speeds ranging from 1000 rpm to 3000 rpm for 60 seconds. The bake temperatures ranged from 100°C to 300°C for 60 seconds.

The developer used was standard 0.26N tetramethyl ammonium hydroxide solution, and the film dissolution rates in developer were measured using both a dissolution rate monitor (DRM) and a spinbowl method. The DRM used in experiment is a Litho Tech Japan model 790, which uses 470 nm light to detect thickness change and the total develop time. The developer temperature was controlled at 21.2°C using a circulation chiller. For the spinbowl test, developer is applied to the wafer for a certain length of time, then rinsed with DI water, and spun dry. The develop rate is calculated by dividing the thickness difference by the develop time.

The silicon dioxide via test wafers, purchased from IMEC, have vias that are 1 μm deep through the silicon dioxide layer and the diameters of the vias used were 0.22 μm. Via holes were patterned at various pitches: dense, semi-dense, and isolated with hole-to-space ratios at 1:1, 1:1. 5, and 1:5. Other via wafers were also used (IMEC), but contain 0.14 μm wide and 0.7 μm deep vias etched into a Black Diamond dielectric layer on a silicon substrate. The cross-sections of all coated via wafers were examined using a scanning electronic microscope (SEM).

Thermal properties were tested on a TA Instruments model 2950 thermogravimetric analyzer with the temperature ramp rate 10°C/min in an air environment.

## 3. RESULTS AND DISCUSSION

### 3.1. Process window

The challenges of designing a developer soluble gap-fill material are that the cured film must be simultaneously soluble in developer and insoluble in organic solvents, and the develop back process has to be well controlled to stop at the via top. Polymers dissolve in solvent in several steps: solvent diffuses into the polymer, polymer swelling occurs, and polymer diffuses into solvent. Each step affects the performance of the gap-fill materials from dissolution rate variation to swelling, peeling, or cracking [6].

The BSI.G05013 polymer has unique properties which make it a suitable developer soluble gap-fill material, the develop rate is easily controlled and it has a very wide bake window. By careful design of the polymer structure, we can easily control the dissolution rate from less than 1 nm/sec to over 100 nm/sec by a simple formulation adjustment. Unlike photoresist, this developer soluble gap-fill material does not utilize photo acid generators as a solubility switch. Instead, it is thermal set during the bake process, which makes the polymer insoluble in organic solvent, but soluble in developer. Most developer soluble materials have narrow process windows because dissolution rate is usually controlled by the extent of cross-linking, which makes it very sensitive to bake temperature. But BSI.G05013 has wide bake window because the curing reaction is nearly complete at the recommended bake temperature, so variations in the bake temperatures have little effect on the extent of reaction.

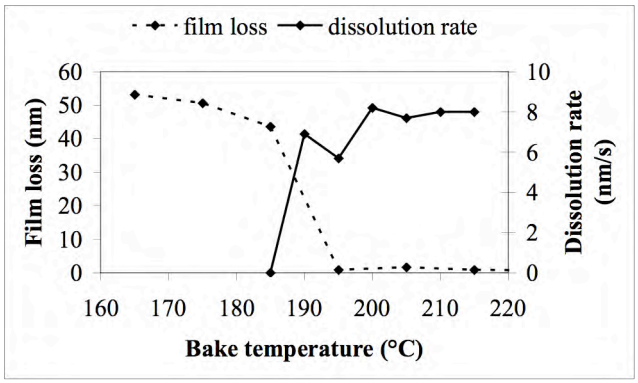



Figure 1. Film thickness loss after PGME/PGMEA mix solvent stripping, and dissolution rate change with bake temperature.

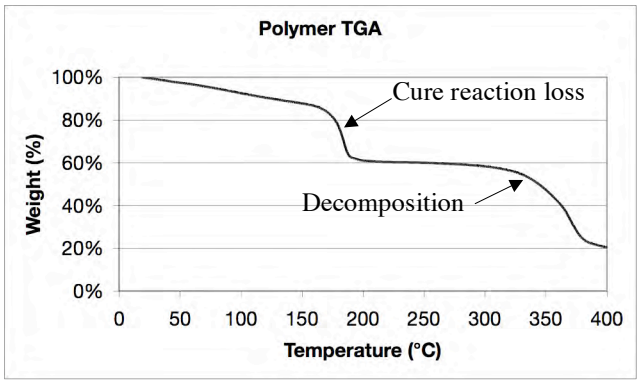



Figure 2. TGA of polymer (temperature ramp 10°C/min in air)

The two plots in Figure 1 show the relationship of film stripping in organic solvent and dissolution rate with changing bake temperature. The transition temperature is clearly seen at 195°C, and baking above this temperature, the film is not stripped in organic solvent and has a constant dissolution rate. The TGA plot in Figure 2 likewise shows this transition. The weight loss from 170°C to 195°C is the loss of small molecular gas generated from curing reaction. The second weight loss around 330°C is polymer decomposition. The flat range between 195°C and 330°C demonstrates a wide process window.

The details of dissolution rate in the range of 200°C to 275°C have been tested on DRM and data is showed in Figure 3. You can see dissolution rate is not a quite constant in this graph. It can be explained by two factors during the bake. One is chemical reaction; the other is solvent evaporation. At higher bake temperature, the reaction completes more, which makes film more soluble, and dissolution rate increasing. However, the higher temperature wafer is baked, the dryer film will form. Solvent evaporation reduces free volume of polymer, which could cause dissolution rate decreases. The model presented in Figure 4 shows dissolution rate is a function of both reaction factor and solvent factor. The total trend forms a low dissolution rate range 200°C to 230°C and high dissolution rate range 240°C to 275°C. But this small change does not affect the other properties of BSI.G05013. Figure 5 is the SEM pictures of BSI.G05013 baked at different temperature after developed back to the via top. The material is very stable, its via fill and develop back property are keep proper up to 275°C. The application temperature we suggest is 200°C to 230°C because this range is commonly used in industry, however, it can be used at higher temperature range as well.

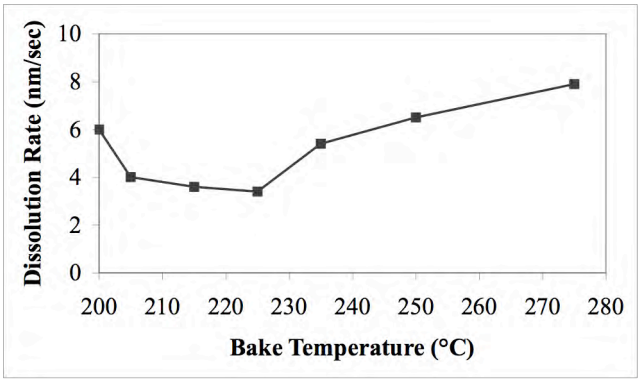



Figure 3. Dissolution rate change with bake temperature.

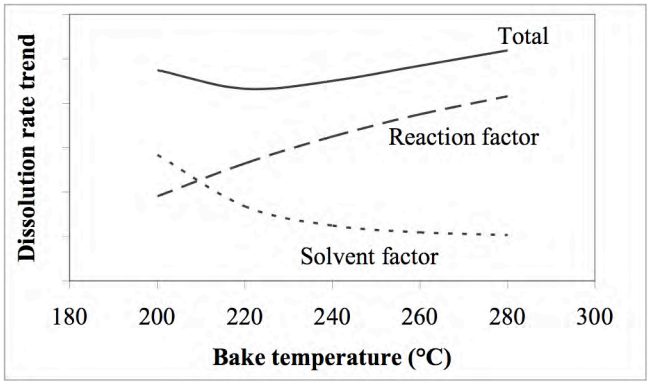



Figure 4. The model of dissolution rate as a function of total of reaction factor and solvent evaporation factor.

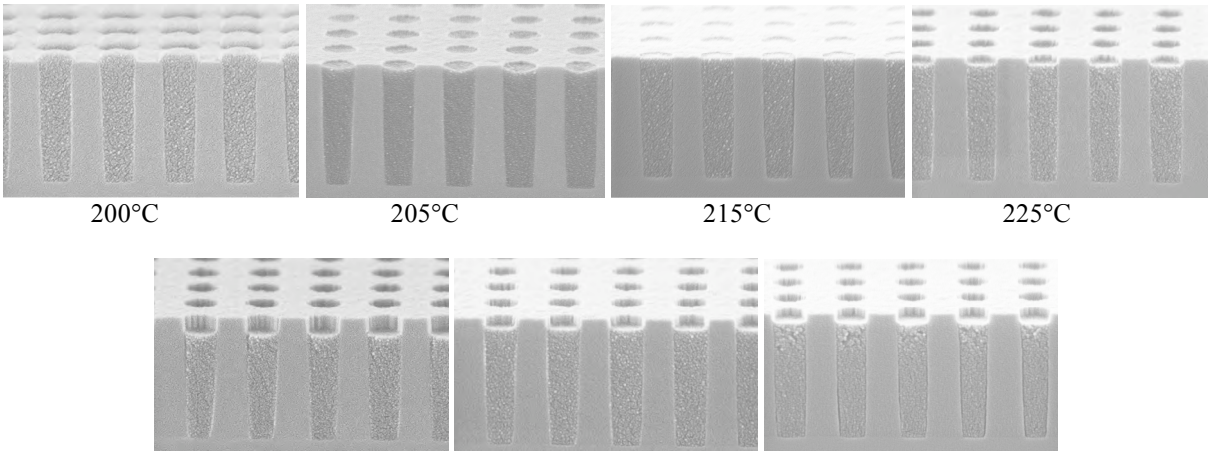



Figure 5. BSI.G05013 is coated on $SiO_2$ via wafer, and baked at different temperature from 200°C to 275°C. The films are etched back to via top in standard developer.

**3.2. Bias reduction**

Spin coating is a common process to distribute material evenly on wafer. However, when the coating is relatively thin and high-aspect features, such as contact holes, are patterned in different pitches, a thickness bias forms between isolated and dense areas [7]. Depending on via size and via distribution, the bias can be a few nm to hundreds nm. Spin coating can also create variation in thickness from the wafer center to edge. This is especially significant with large wafer sizes and low spin speeds. Our BSI.G05013 material can reduce the local and global bias dramatically because the dissolution rate of the material inside of vias is slower than the dissolution rate of bulk material [6]. Figure 6 shows cross-sections

of BSI.G05013 coated on via substrates before and after developer etch-back. The bias of isolated and dense areas before develop back is 250 nm (Figure 6a). After 69 seconds of develop back (Figure 6b), the open area and the surface between vias areas are clear. The gap-fill material fully fills the isolated vias and it is only 50 nm below via surface in the dense area. Once the material is developed to the via surface, dissolution rate begins to decrease. This is shown by increasing the develop time by 19 seconds, whereas both the fill and bias did not change considerably (Figure 6c). This attribute provides a large time control margin to process BSI.G05013.

Measurements of the SEM pictures Figure 6 gives the dissolution rates of BSI.G05013 above and inside of the vias (Figure 7). Measurements were performed by considering the via top as zero, material above the via top is considered a positive thickness, and below the via top is negative thickness. The slopes of the trend lines present average dissolution rates at dense, isolated, and open areas, which are 5.64 nm/s, 3.64 nm/s, and 1.57 nm/s, respectively. This average dissolution rate difference is the main reason of significant bias reduction.

a) Non develop

b) Develop 69s

c) Develop 88s

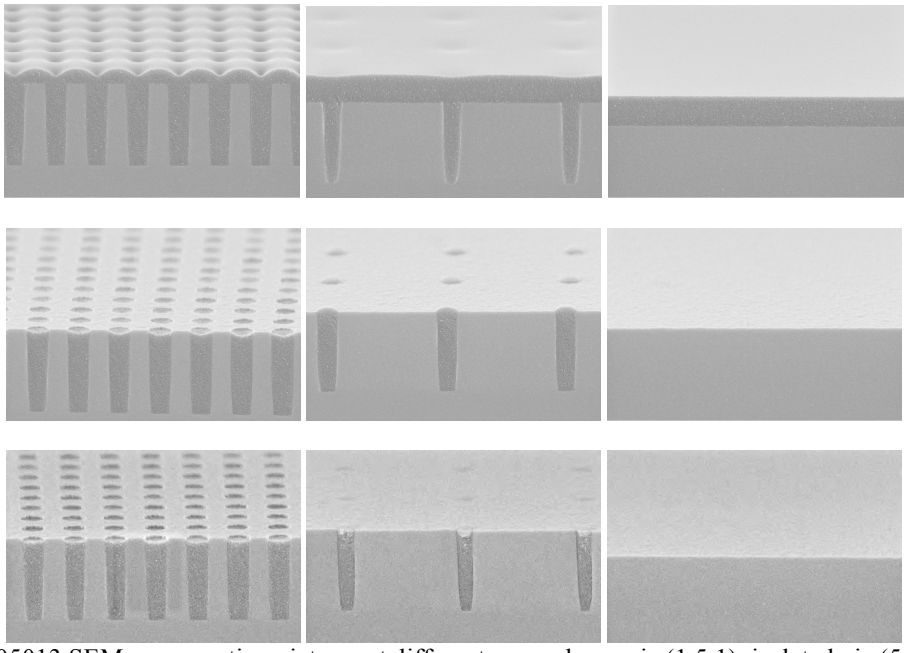


Figure 6. BSI.G05013 SEM cross-section pictures at different areas, dense via (1.5:1), isolated via (5:1), and open, on $SiO_2$ via wafer. a) no develop, b) develop 69s, c) develop 88s.

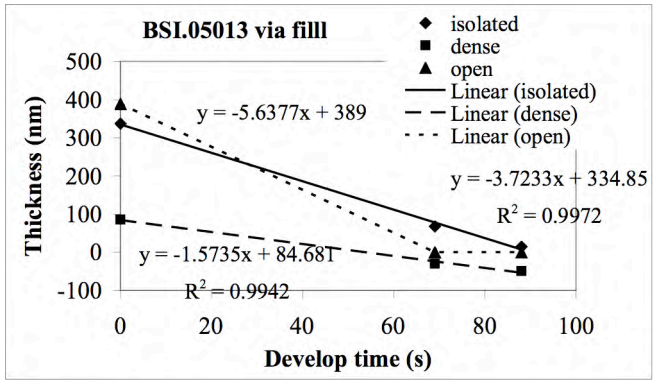



Figure 7. The measurement from SEM cross-section in Figure 6.

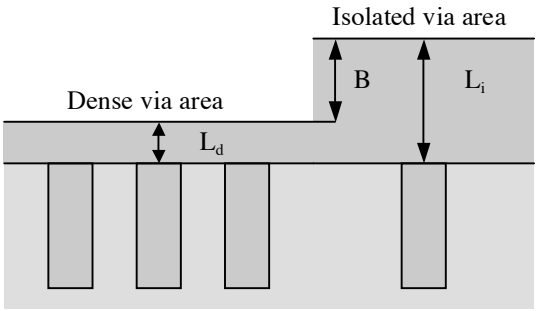



Figure 8. Scheme of thickness measurement.

The difference in dissolution rates can be use to form a bias reduction model. Figure 8 represents the initial coating, where $B$ is initial bias, $b$ is final bias, $R_b$ is the dissolution rate of bulk material, $R_v$ is dissolution rate of the material in the vias, and $t_{develop}$ is develop time. From this, the bias can be expressed as:

$$t_{develop} = \frac{L_i}{R_b} = \frac{L_d}{R_b} + \frac{b}{R_v}$$

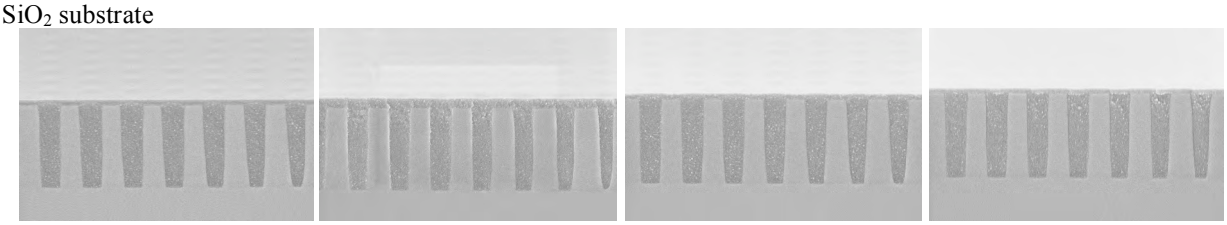
$$\frac{B}{R_b} = \frac{b}{R_v} \quad \text{or} \quad \frac{B}{b} = \frac{R_b}{R_v}$$

Assuming $L_i >> L_d$ on the IMEC via substrate and $R_b >> R_v$ for BSI.G05013 material, the average dissolution rate at dense area is close to the dissolution rate in via $R_v$ and dissolution rate at open area is close to the dissolution rate of bulk material $R_b$. Therefore, the bias reduction ratio should be 5.64/1.57=3.59, so it should be possible to reduce bias by 3.59 times on any via substrate using the BSI.G05013 gap-fill material and the develop back process.

**3.3. Substrate and BARC compatibility**

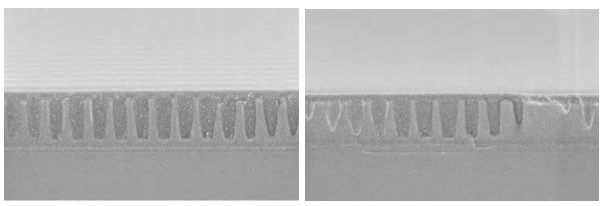
With the continually shrinking semiconductor feature sizes, the distance of interconnect metal lines becomes closer. To conquer the cross talking problem, many kinds of low-k dielectric materials have been developed besides $SiO_2$. BSI.G05013 had been used to fill different via substrates, such as Fluorinated Spin-on Glass and Black Diamond, and provides the same develop properties and without void formation.

a) $SiO_2$ substrate



BSI.G05013/ARC29A BSI.G05013/ARC82A BSI.G05013/DUV42P BSI.G05013/DUV42P

b) Black Diamond substrate

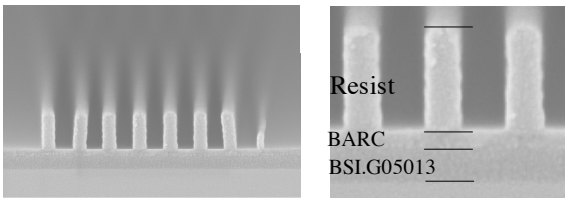


BSI.G05013/ARC29A BSI.G05013/DUV42P

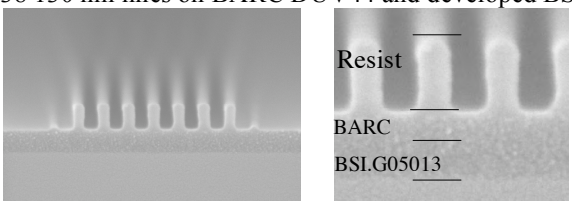
Figure 9. BSI.G05013 applied on $SiO_2$ and Black diamond via substrates with different BARCs on the top.

Also, it is compatible with BARCs for different wavelength lithography applications. Figure 9 shows BSI.G05013 on two kinds substrates, $SiO_2$ and Black Diamond, and Brewer Science ArF BARCs (ARC29A and ARC82A) and KrF BARCs (DUV42p and DUV44). The gap-fill material was developed to the via surface and the 60 nm to 90 nm layer of BARC was applied to the top. The surfaces are perfectly flat, and no void formed in the vias.

In the situation of developing to the top of vias, resist lines should stand on the surface between vias, where gap-fill material is clean. To be sure of no interaction between gap-fill material and the top layer materials, we performed resist lithography with 100 nm thick BSI.G05013 remaining under the BARC. Three layers above silicon substrate can be seen from the pictures in Figure 10: the top layer is resist lines, the second layer is a BARC layer, and the third layer is BSI.G05013. The resist profile is straight and the depth of focus is broad. The resist lithographic performance is as good as on BARC/Si alone.




a) KrF resist P338 130 nm lines on BARC DUV44 and developed BSI.G05013 stack




b) ArF resist AR1682J 80 nm lines on BARC ARC29A and developed BSI.G05013 stack

Figure 10. Resist profiles on BARC and developed BSI.G05013 stack, a) KrF lithography, b)ArF lithography.

**3.4. Stability**

BSI.G05013 is a very stable product. The two months of aging data in Figure 11 shows no change on thickness or dissolution rate. The accelerated aging test at 35°C also did not show any change.

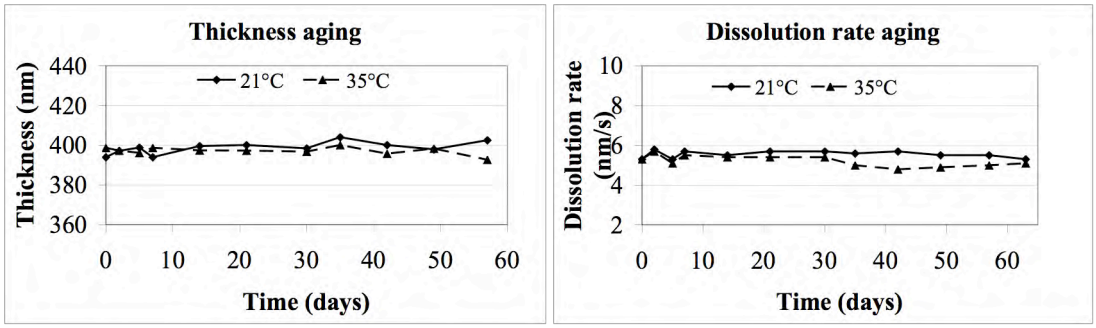



Figure 11. Two month aging stored at room temperature and 35°C.

**3.5. Spinbowl and solvent compatibility**

In spin coating process, polymer residue dried in the spin bowl and surround the nozzle must be cleaned by solvents periodically to keep track clean and reduce defects source. We perform spinbowl compatibility tests for this purpose. Wafers are coated and stored open at room temperature for one day to simulate the spinbowl drying condition. Then solvent strip tests carried out and >90% loss represents material spinbowl compatibility. BSI.G05013 is compatible with

the solvents commonly used in semiconductor industry, such as PGMEA, PGME, ethyl eactate, acetone, cyclohexane, heptanone, and edge bead cleaners.

## 4. CONCLUSION

The BSI.G05013 developer soluble etch-back gap-fill material developed at Brewer Science provides excellent via fill, isolated and dense bias reduction, and wide process windows. Therefore a wet etch-back gap-fill DD process may provide a better alternative to the currently used plasma etch-back gap-fill process to achieve planar surfaces required for trench lithography. The developer etch-back gap-fill process allows coating, baking, and etch-back to be done in the same track, which eliminates the need to transfer wafers between the etch and photo bays, which increases throughput, reduces defects, and makes the process more cost-effective.

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