ECS Transactions, 18 (1) 419-425 (2009)
10.1149/1.3096480 ©The Electrochemical Society

# Residue Testing of Developer-Soluble Bottom Anti-Reflective Coatings

Carlton Washburn, April Evers, and Brian Smith

Brewer Science, Inc., Rolla, MO 65401, USA
cwashburn@brewerscience.com

Organic developer-soluble bottom anti-reflective coatings (DBARCs) are commonly used in the photolithographic process for implant and high-k/metal gate integration. They provide added reflectivity control over topography compared top anti-reflective coatings (TARCs). DBARCs are coated onto substrates and then removed during the develop step with the resist. Occasionally a thin post-develop residue (PDR) remains after the DBARC removal process. The main drivers of this residue are DBARC bake temperature, followed by develop time. For this investigation the amount of residue was tested using Si, $SiO_2$, native $SiO_2$, SiN, and $HfO_2$ substrates at different bake temperatures. In addition, contact and proximity baking are compared and shown to be equivalent in terms of their effect on PDR. This work demonstrates that optimizing the bake process of a DBARC is an effective way to control PDR on a variety of substrates.

## 1.0 Introduction

As integrated circuit (IC) technology advances, the materials used in manufacturing become more sophisticated. As materials advance, the processing required to optimize and qualify the materials becomes more complex. The photolithography process engineer in particular faces many challenges while selecting and using resists and anti-reflective coatings. This complexity places more pressure on the process engineer to develop processes that are both robust and cost-effective. There are now several different types of resists, hardmasks, gap-fill materials, underlayers, and bottom anti-reflective coatings (BARCs). BARC varieties include traditional dry-etch, wet-developable, graded index, and silicon-containing (1,2,3,4).

Process development for developer-soluble bottom anti-reflective coating (DBARC) materials is distinctly different from that for traditional dry-etch BARCs (5). Dry BARC process development is straightforward and has fewer variables. Once resist compatibility is established, the remaining issues involve mainly thickness, etch selectivity, and defect concerns (6). DBARC process development must take into account many additional concerns such as the choice of thermosetting or photosensitive materials (5), as well as the control of post-develop residue (PDR), which can vary depending on the substrate, and is the focus of this investigation.

Two typical applications for DBARC are in ion implantation and high-k/metal gate (HKMG) patterning. These applications can be negatively affected by PDR unless methods exist to characterize the process at an early stage. Understanding the causes of residue and its impact on processing can help to reduce integration problems.

Understanding what steps to monitor becomes critical to maintaining a stable process. This paper will show that by use of process optimization, PDR with thermosetting DBARC can be minimized. It will further evaluate how this can be applied to different substrates common to implant and HKMG applications.

## 2.0 Experimental Method

The method used to evaluate PDR was based on spectroscopic ellipsometry (SE). Using an M-2000® SE from J.A. Woollam Co., the process begins with a measurement of the native oxide or inorganic film thickness on the substrate. Next, the DBARC, Brewer Science™ ARC® DS-K101 coating, was dispensed onto the wafer. Cauchy coefficients of the DBARC were then recorded from the SE and the wafer was developed in 0.26N TMAH with a surfactant (7). Finally, the substrate was measured again with the SE. These measurements were used to build a model that looks for subtle changes in the polarization of the light that would be caused by a residue. If a residue was found, then the average thickness was calculated.

$SiO_2$, native $SiO_2$, SiN, and $HfO_2$ substrates were used for this study because they are representative of some of the surfaces encountered in implant and high-k/metal gate lithography. DBARC was dispensed onto 200-mm wafers by hand using a TEL Mark 8 Clean Track coater system with HHP proximity bake plates. The develop process used an $E^2$ developer nozzle. Also, 100-mm wafers were hand-coated and processed using a Brewer Science™ Cee® 200CB system and a contact bake plate. Typical bake conditions were 185°C for 60 seconds, followed by developer-rinse for 60 seconds, and final deionized water rinse.

Factors that can contribute to residue were screened and modeled with a design-of-experiments (DOE) approach. Stat-Ease's Design Expert® version 7.0.1 software was used for DOE design and analysis. DOE is a statistical tool that allows screening of effects from multiple factors more efficiently then by testing one factor at a time. Fractional factorial DOE designs offer a straightforward approach for evaluating main effects and some two-way interactions, while follow-up response-surface DOEs provide detailed information on the best locations to optimize a process.

## 3.0 Results and Discussion

Using the SE method, six process factors and one chemical loading factor that adjusts develop rate were evaluated as possible residue drivers. A resolution-IV fractional factorial DOE was used to screen for the drivers which had the greatest impact on PDR. The design is detailed in Table 1. Because the goal was to screen a large number of factors 100-mm substrates were used initially for speed and convenience.

**TABLE I**. Factors utilized in the DOE.

| Factor | Unit | High | Low |
|---|---|---|---|
| Bake Temp | (°C/60 s) | 205 | 135 |
| Bake Time | (s) | 105 | 15 |
| Develop Time | (s) | 120 | 30 |
| Film Thickness | (nm) | 290 | 750 |
| Exposure | (mJ/cm$^2$) | 60 | 0.0 |
| Develop Puddles | (#) | 1 | 4 |
| Develop Rate | (ratio) | High ratio | Low ratio |

The resulting PDR data were processed using Design Expert®. The half-normal plot is shown in Figure 1. Bake temperature had the greatest effect, with bake time and develop time having lesser effects. These three factors were used to design a central composite response-surface DOE to map out the factor interactions and to generate and study trends.

The response-surface DOE was run twice, once on 100-mm contact-baked substrates and again using 200-mm proximity-baked wafers. Because bake temperature was determined to have the greatest impact on PDR, the goal was to compare the resulting response surfaces to determine whether or not there was a difference in trends from the two different heat transfer modes. A second goal was to gauge any processing offset between contact and proximity-baked wafers. Results of the two DOEs are shown in Figure 2. The curvature of the surfaces shows that the trend for both experiments was the same. Higher bake temperatures increase PDR. Also, develop time had an interaction with bake temperature. At very high bake temperatures and short develop times, the remaining BARC film increased rapidly. This result was not so much a function of residue, rather incomplete development of a highly crosslinked film. Chemically the degree of crosslinking increases with an increase in bake temperature, but not necessarily bake time, as with Arrhenius behavior. This is confirmed by the relatively insignificant effect of bake time, which is not shown.

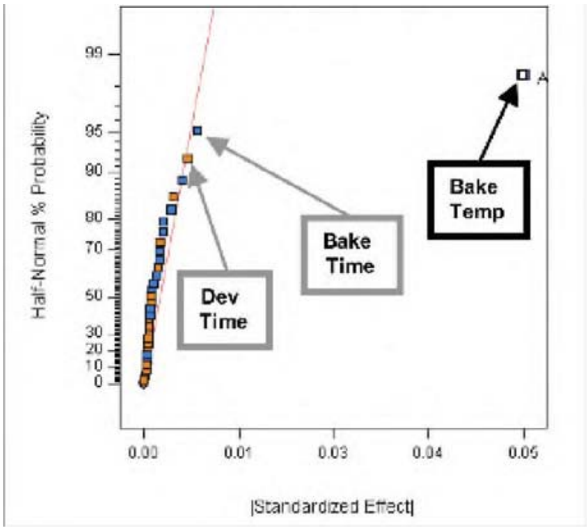
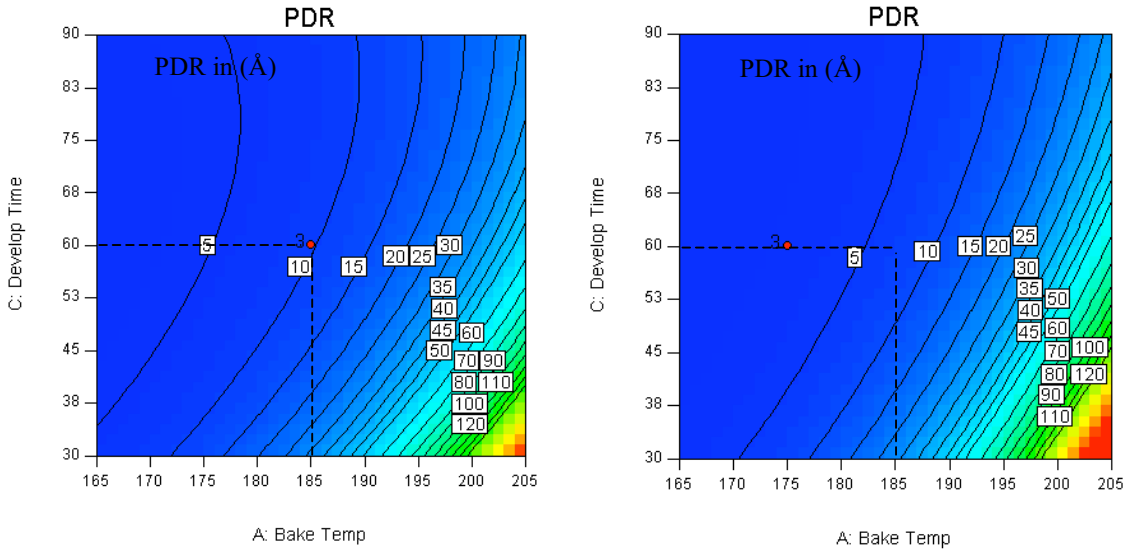



**FIGURE 1.** Factorial DOE half-normal plot.

A slight offset occurred between the center of the two surfaces, which is shown by the dashed lines in Figure 2. The standard deviation of the replicated center points for the 100-mm DOE was 0.6 Å, and for the 200-mm track process DOE the standard deviation was 0.3 Å. Thus the offset between the two response surfaces is beyond the experimental error and is real. This offset likely came from a difference in temperatures between the two hot plates used. Because different bake temperatures were used during the testing, hot plate equilibrium times may not have been sufficient. This is the likely source of offset between the two tests.




200-mm proximity baked 100-mm contact baked

**FIGURE 2.** DOE response surface plots of PDR.

To confirm the 200-mm DOE results, additional wafers were processed. The develop time and bake time were both held constant at 60 seconds. Then the resulting PDR data were plotted against the DOE model to confirm the model (Figure 3). The model and empirical data match well up to 180°C, at which point they separate, then recombine near 205°C. This mild deviation is expected from comparing the model fit against the new, more complete data set, and this confirmation was considered successful. It also showed that optimizing DBARC bake temperature can minimize PDR. This will improve HKMG and implant applications that are sensitive to residue.

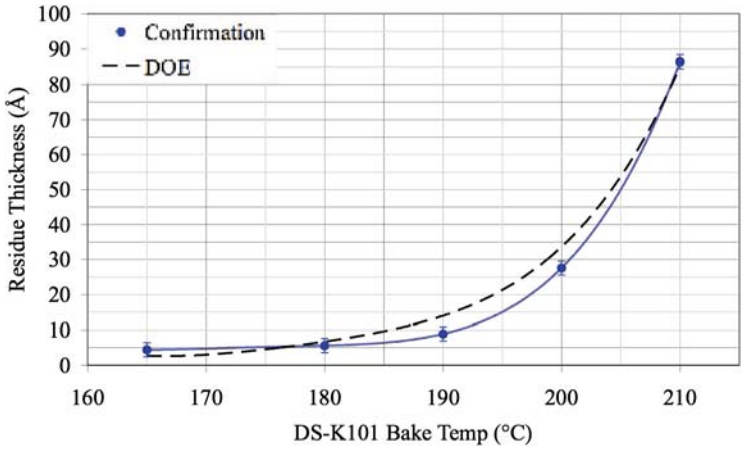



**FIGURE 3.** Bake confirmation of 200-mm track-processed wafers.

Previous testing has shown that photosensitive DBARCs have different amounts of PDR when processed over silicon compared to silicon dioxide (7). To further the understanding for the thermosetting DBARC (ARC® DS-K101 coating), similar testing was performed. Silicon and 200 nm of $SiO_2$ were tested to compare to previous photosensitive DBARC data. 300 nm of SiN and 7 nm of $HfO_2$ were also tested. The results are shown in Figure 4. By far, SiN showed the most residue. SiN is well known interact with organic resist layers to cause scumming problems due to the residual N-H bonds that neutralize the acid in chemically-amplified resists (8). A similar mechanism may be at work in the case of DBARC, resulting in a neutralizing of the base-soluble components at the DBARC/nitride interface. Residue thickness from $HfO_2$ was half that of silicon, with $SiO_2$ showing the least amount of residue. The reduced residue result with $SiO_2$ aligns with previous results from photosensitive DBARC testing (7).

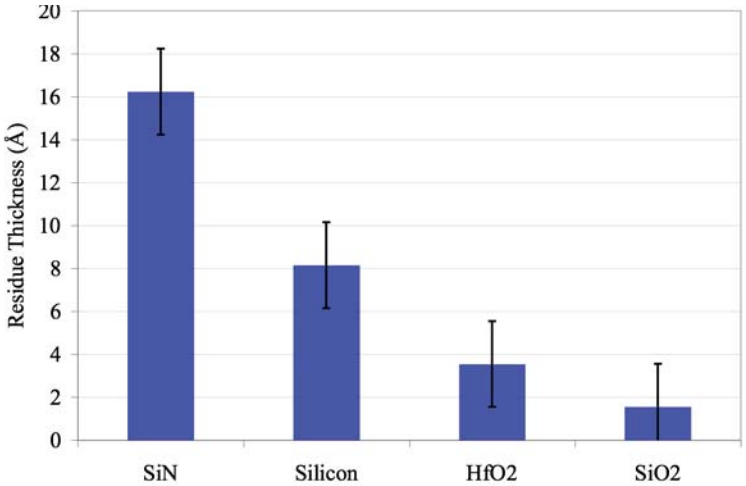



**FIGURE 4.** PDR on different substrates.

To further explore the relationship between $SiO_2$ substrates and residue, the native oxide of a silicon wafer was mapped, then ARC® DS-K101 coating was applied to the wafer and developed away. These results are shown in Figure 5. A linear trend resulted, indicating that increases in native $SiO_2$ produce less PDR. The proposal that a thick film of $SiO_2$ would decrease the surface silicon sites available for DBARC to bind to was previously proposed (7). This concept was supported by these results in that as the native oxide increases, it may become less and less ordered like pure silicon.

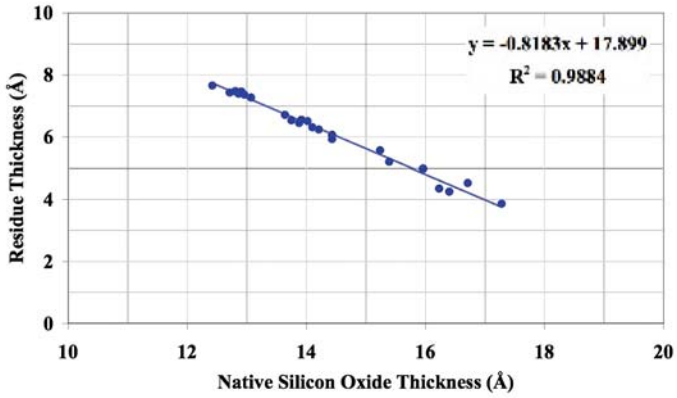



**FIGURE 5.** PDR on various thickness of native $SiO_2$.

## 4.0 Conclusions

To summarize, a factional factorial DOE was designed to screen several processing and one chemical factor for residue using ARC® DS-K101 coating, a thermosetting DBARC. It was learned that bake temperature was the main driver. Two response-surface DOEs were then designed to further investigate baking as a residue driver. Bake temperature was confirmed to be the largest driver, followed by an interaction with develop time. This showed that optimizing DBARC process conditions can minimize PDR for applications including HKMG and implant patterning.

Substrate testing showed SiN to have the largest effect on residue, followed by Si, $HfO_2$, and $SiO_2$, which showed the least residue. Native $SiO_2$ was tested and showed a linear trend of decreasing PDR with an increase in native oxide.

## 5.0 Acknowledgments

The authors would like to thank Brandy Carr for her wafer processing assistance. The authors would also like to thank Andrea Fuchser of J.A. Woollam Co. for her advice and support during this study.

## 6.0 References

1. Xie Shao, Alice Guerrero, and Yiming Gu, "Wet-Developable Organic Anti-Reflective Coatings for Implant Layer Applications," SEMICON China 2004 SEMI Technology Symposium, March 17-19, 2004.

2. S. Lee, J. Jung, S. Cho, C.Lim, C. Bok, H. Kim, S. Moon, J. Kim, *Proceedings of SPIE*, Vol. 6153, 2006.
3. S. Burns, D. Pfeiffer, A. Mahorowala, et al, *Proceedings of SPIE*, Vol. 6153, 2006.
4. D. Goldfarb, S. Burns, L. Vyklicky, et al, *Proceedings of SPIE*, Vol. 6923, 2008.
5. C. Washburn, A. Guerrero, R. Mercado, D. Guerrero, J. Meador, *INTERFACE 2006: Proceedings of the 43rd Microlithography Symposium*, 2006.
6. A. Gabor, S. Halle, C. Kallingal, *Proceedings of SPIE*, Vol. 5753, 2005, pp. 699-707.
7. D. Guerrero, J. Lowes, R. Mercado, *Journal of Photopolymer Science and Technology*, Vol. 20, no. 3, 2007, pp. 339-343.
8. J. Chun, C. Bok, K. Baik, *Journal of Photopolymer Science and Technology*, Vol.10, no.3, 1997, pp.445-450.