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Foundry Efficiency Gains Through Common Photolithography Themes

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Here we examine photolithography methodologies to improve the efficiency of foundry and ASIC manufactures that have many part numbers with relatively low run volumes. In such cases, a fab must accommodate a large variety of device layers, topography dispersion, and layout parameters. These factors reduce the lithography process margin and limit design freedom and throughput in the lithography module. These factors also increase design complexity, optical proximity correction (OPC) design loops, mask cost, exposure dose, and number of material sets to meet layer requirements. Consequently, these factors impact the fab's overall efficiency. The primary method proposed to improve efficiency is to use a system that includes a planarizing etch transfer layer, an image transfer layer, and an image capture layer. By combining these elements, the lithography process becomes very predictable, simple, and repeatable, independent of the device.

1. Introduction

In this paper, we examine photolithography methodologies to improve the efficiency of foundry and ASIC manufactures that have many part numbers with relatively low run volumes. In such cases, a fab will need to accommodate a large variety of device layers, topography dispersion, and layout parameters. In turn, these factors reduce the lithography process margin, limit design freedom, and reduce throughput in the lithography module. At the same time, these factors increase design complexity, optical proximity correction (OPC) design loops, mask cost, exposure dose, and the number of material sets required to meet individual layer needs. Thus the above items impact the overall efficiency of the fab.

2. Theory and Simulation of Lithography Latitude

Lithography performance strongly depends on stack design. Often the substrate has a variety of topography, transparent dielectric layers, and multiple patterned device layers with a wide range of reflectivity. This situation leads to a wide range of topography and reflectivity dispersion that makes conventional lithography difficult, consuming much of the CD processing window.

Figure 1 represents a stack with different SiO_2 thicknesses on the same wafer. The bottom anti-reflective coating (BARC, ARC® 29 material) and the resist are assumed to be conformal coatings.

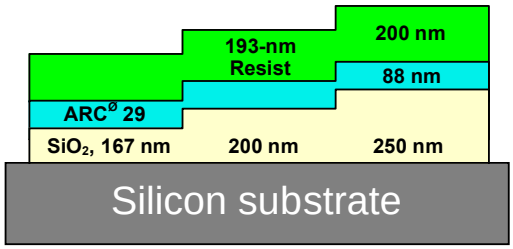


Figure 1. Lithography stacks on substrate with topography.

Figure 2 is the substrate reflectivity (%R) varying with oxide thickness simulated with PROLITH v11. The substrate reflectivity is 5.1% for an oxide thickness of 167 nm, 0.35% for a 200-nm thickness, and 2.1% for a 250-nm thickness. Thus, the lithography step is performed under very different optical conditions due to the underlying stack and topography. Even with a small change in oxide thickness from 200 nm to 235 nm, the reflectivity would change from 0.35% to 5.1%, leading to little or no process latitude.

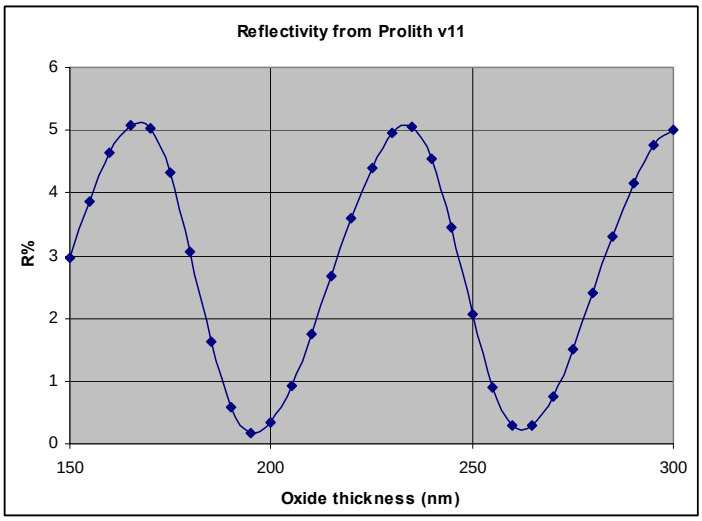


Figure 2. Substrate reflectivity varies with oxide thickness when using a single-layer BARC process.

Figure 3 shows the CD processing window simulated with PROLITH v11. These simulations are based on an ASML 1100 (ArF) scanner with settings of NA = 0.75, dipole 35Y, sigma = 0.89/0.65, and an 80-nm 1:1 mask. It is obvious that both windows shifted from each other in both depth of focus (DoF) and exposure dose, resulting in a smaller common window (dashed black lines).

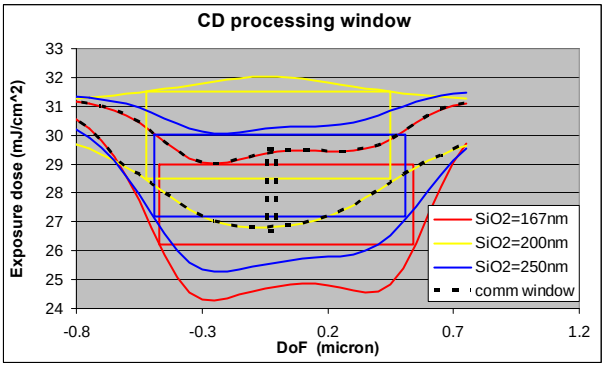


Figure 3. CD processing window: red for 167 nm, yellow for 200 nm, and blue for 250 nm of SiO_2 thickness; black dashed line is the resulting common window.

Figure 4 is the exposure latitude with respect to DoF. If the exposure dose tolerance is set at ± 5%, then the individual stacks have a wide DoF, (~1000 nm). However, the DoF will shrink to zero, as shown with the black curve, if all three stacks receive the same exposure dose.

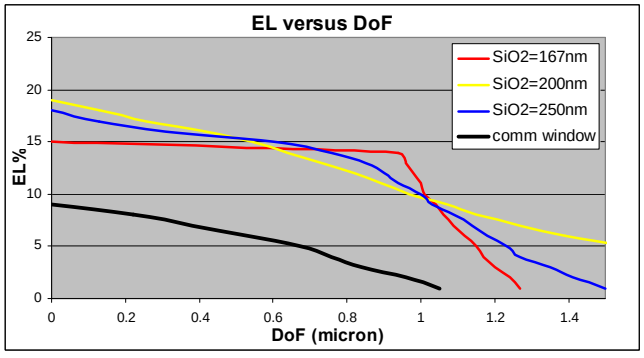


Figure 4. Exposure latitude with respect to DoF.

In this paper we recommend a multilayer patterning system, the OptiStack® system, as shown in Figure 5. In this figure, the etch transfer layer has four functions: topography planarization, optical isolation, high-aspect-ratio pattern transfer, and an easily strippable film following substrate etch transfer or implant. The second layer is a pattern transfer layer that has two key functions: transfer of a low-aspect-ratio organic image layer pattern into a high-

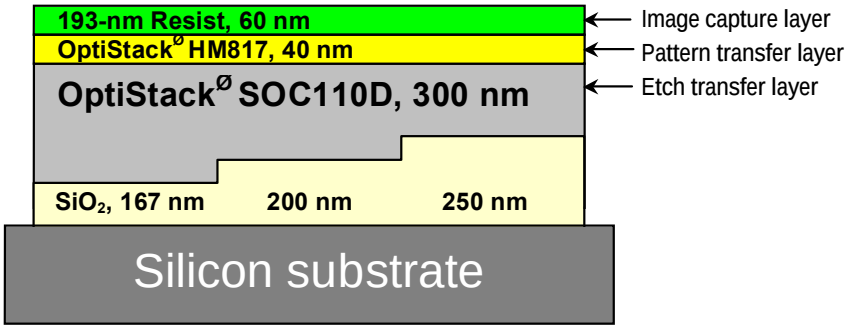
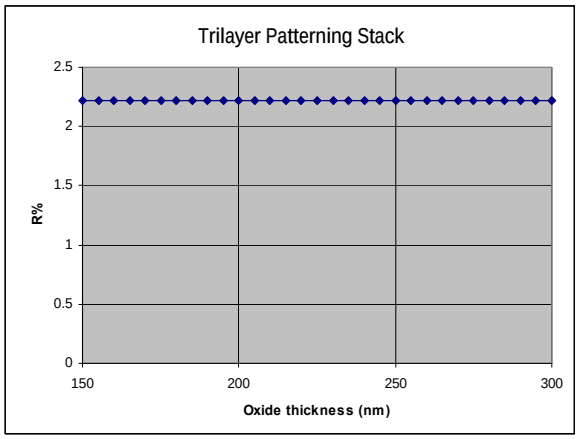


Figure 5. Recommended OptiStack® patterning stack.

aspect-ratio organic resist transfer layer and tuning of the ideal optical surface for lithography fidelity and process latitude. The top image capture layer is a thin version of a typical photoresist that has the primary purpose of capturing the lithography image and the ability to transfer that image by plasma etching into the thin pattern transfer layer. Thickness of the image capture layer is less influenced by the substrate topography, and, most importantly, the UV distribution is absolutely independent of the substrate reflectivity dispersion. Figure 6 is the reflectivity curve versus SiO_2 thickness. The oxide thickness does not change the optical property of the stack due to the isolation of the high-k OptiStack® SOC110D layer. In this case, the CD processing window will be identical over the entire topography of the wafer. Another big advantage of such a stack is that the image capture layer thickness is free of etch budget requirements and can be optimized for the maximum CD processing window.



By eliminating reflectivity dispersion and minimizing topography dispersion, the user of the OptiStack® system can process with a common substrate independent of the device layer. The two key variables for any device layer are 1) the thickness of the etch transfer layer to meet the required aspect ratio for either etch or implant of the substrate layer and 2) the required etch transfer process to transfer the image into the pattern transfer layer. The implication is that the top two layers of the system are identical, independent of device layer or device type, thereby greatly simplifying the exposure and develop steps. This simplicity will have its greatest effect by allowing wide process margins, which in turn allow opening the design rules for a given exposure tool set operated by a fab. This simplicity also allows OPC to be calculated directly and incorporated into the design rules so no reiterative mask designs are needed for OPC feedback. All learning at any device layer can be applied to any and all other layers for the particular exposure tools used. Another advantage of implementing the parameters identified by the OptiStack® system would be a reduction in the overall number of materials that could be used across all devices and device layers, with only the etch transfer layer thickness varying as needed to achieve the planarization and aspect ratio required. Meeting these requirements would typically add one process layer per wafer and call for the additional etch capacity required for dry-etch pattern transfer. The impact on cost will be discussed in Section 4.

3. Experimental Validation

The lithography experiment for the two stacks shown in Figure 1 has been done at IMEC with ASML 1100 (ArF). Table I lists the experimental conditions.

Table I. Lithography conditions.

Parameter	Conditions
Resist:	**AR1682J-15**
Resist thickness (nm):	200
Resist coat (rpm/s):	1100/30
Target CD (nm/pitch):	80L/160P
PAB (□C/s):	110/90
Illumination mode:	Dipole35Y
NA:	0.75
Sigma (outer / inner):	0.89 / 0.65
Center dose/step (mJ/cm ^{2}):	26 / 1
Focus offset/step (μm):	0 / 0.1
Reticle bar code:	TM99YCK%L1%M
PEB (□C/s):	110/90
Developer type/time (s):	OPD262/40

Figure 7 shows the results of top-down CD measurement, and Figure 8 shows the CD processing window. At ± 5% exposure dose tolerance, 200-nm SiO_2 has a 465-nm DoF, and 250-nm SiO_2 has a 585-nm DoF. The overlap of these two CD windows leaves 375 nm. Both simulation and experiment show the CD processing window shrinkage by substrate reflectivity variation.

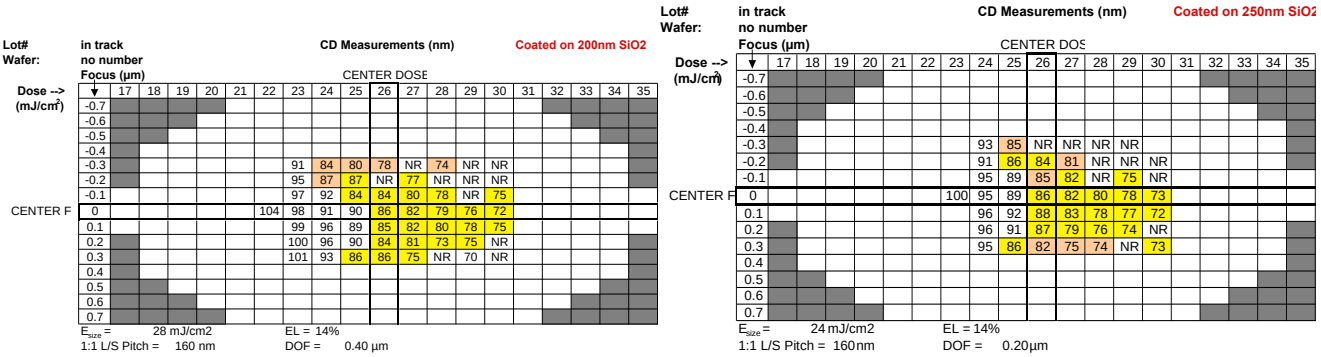


Figure 7. Focus and exposure matrix of top-down CD measurement results.

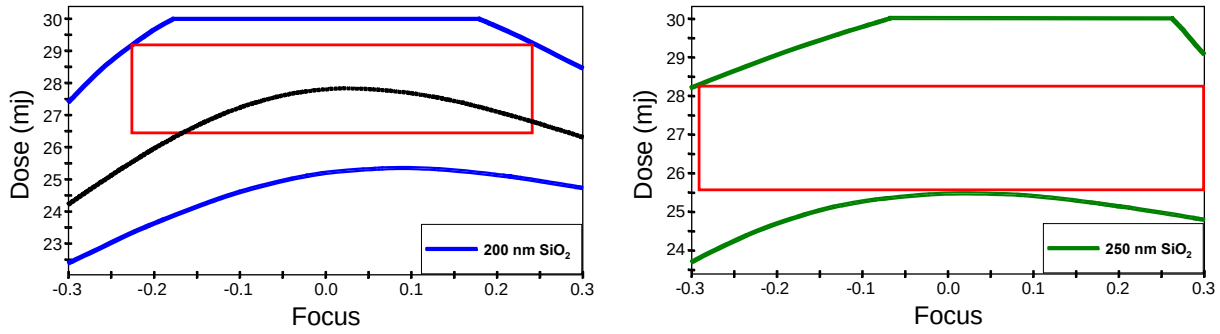


Figure 8. CD processing window. The graph at left is for the 200-nm SiO_2 thickness, and the graph at right is for the 250-nm thickness.

4. Cost of Ownership

Cost of ownership plays an important role in process materials and methods decisions. Process simplifications brought about by layer-to-layer synergy drive significant cost of ownership advantages for the OptiStack® system. Savings in mask engineering and manufacture are the greatest cost difference. OPC algorithms need only be determined once for all layers, rather than individually for each layer, which results in fewer mask corrections. Advanced devices with smaller critical dimensions benefit most from this system in that there are more layers at smaller critical dimensions, requiring greater mask design and production costs.

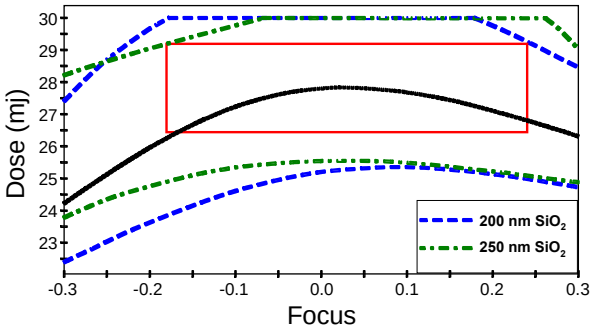


Figure 9. Overlap of CD processing windows.

For the purpose of providing a cost of ownership estimate, we compared a process using the OptiStack® system on eight layers to a typical dyed resist process. Note that the OptiStack® system process would use the same OPC algorithm on all layers. More layers utilizing the same system will result in greater savings. We assumed that 2500 wafers [1] would be printed from each mask; this is said to be a typical usage - ASIC masks may be imaged on as few as 500 wafers. Mask design and mask production are the significant cost components in any analysis of lithography process cost of ownership [5]. For a high-performance mask set with 90-nm design rules, individual binary chrome-on-glass masks can cost $100,000 to produce, and phase shift masks can cost as much as $124,000 [6]. As a conservative estimate, the average mask cost was taken to be $70,000 because some layers can be printed using DUV tools and masks. Accounting for these and other costs, the OptiStack® system saves about $674 per wafer. The cost comparison is shown in Table II. “Other Optistack system costs” are caused by additional materials and processing. These are detailed for processing eight layers per wafer in Table III.

Table II. Cost of ownership comparison.

Mask Design		
Mask design cost	$	102,300
Layers per process converting to OptiStackØ system		8
Mask trials		2.25
Dyed resist mask design	$	3,682,800
OptiStackØ system mask design	$	2,659,800
Difference	$	(1,023,000)
Mask Production		
Mask production cost	$	70,000
Mask trials		2.25
Dyed resist mask production	$	2,520,000
OptiStackØ mask production	$	1,820,000
Difference	$	(700,000)
Wafer images per mask		2500
Design cost (savings) per wafer	$	(409)
Mask production cost (savings) per wafer	$	(280)
Other OptiStackØ system costs	$	86
OptiStackØ system net cost (savings)	$	(603)

Table III. Additional materials and processing cost versus single-layer resist.

Etch transfer material spin-on	$	25	New spin capacity and material
Pattern transfer material spin-on	$	15	New spin capacity and material
Spin on thin resist	$	(6)	Less material used
Resist pre-exposure bake	$	(3)	Less time due to thinner layer
Resist expose	$	(14)	Shorter exposure time
Resist post-exposure bake	$	(3)	Less time due to thinner layer
Etch transfer layer etch	$	36	Additional etch
Pattern transfer layer etch etch	$	36	Additional etch
Total cost per wafer	$	86	8 layers per wafer

Using this type of multilayer system is likely to bring even more benefits to the overall fab cost and efficiency. Other areas to be studied in future work are the impact of simplified inventory arising from the need for fewer custom materials by layer or device.

5. Conclusion

By combining these elements of the OptiStack® system, the lithography process becomes very predictable, simple, and repeatable, independent of the device. OPC can be well characterized and applied uniformly to all process layers in a single pass, reducing both the cost of design and mask-making loops. A single image capture layer and image transfer layer system can be used on all device layers for each exposure tool generation. Simply varying the thickness of the planarizing etch transfer layer achieves the aspect ratio needed for substrate etch transfer or implant protection. With the low-aspect-ratio image capture layer, process margins are greatly expanded, which potentially allows fabs with lithography tool limitations to expand their design rules to cover added device designs. Work will be continued to more fully identify the impact on overall fab efficiency and cost and to perform process testing to map the fab or ASIC manufactures conditions that can best take advantage of this technology.

Acknowledgments

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