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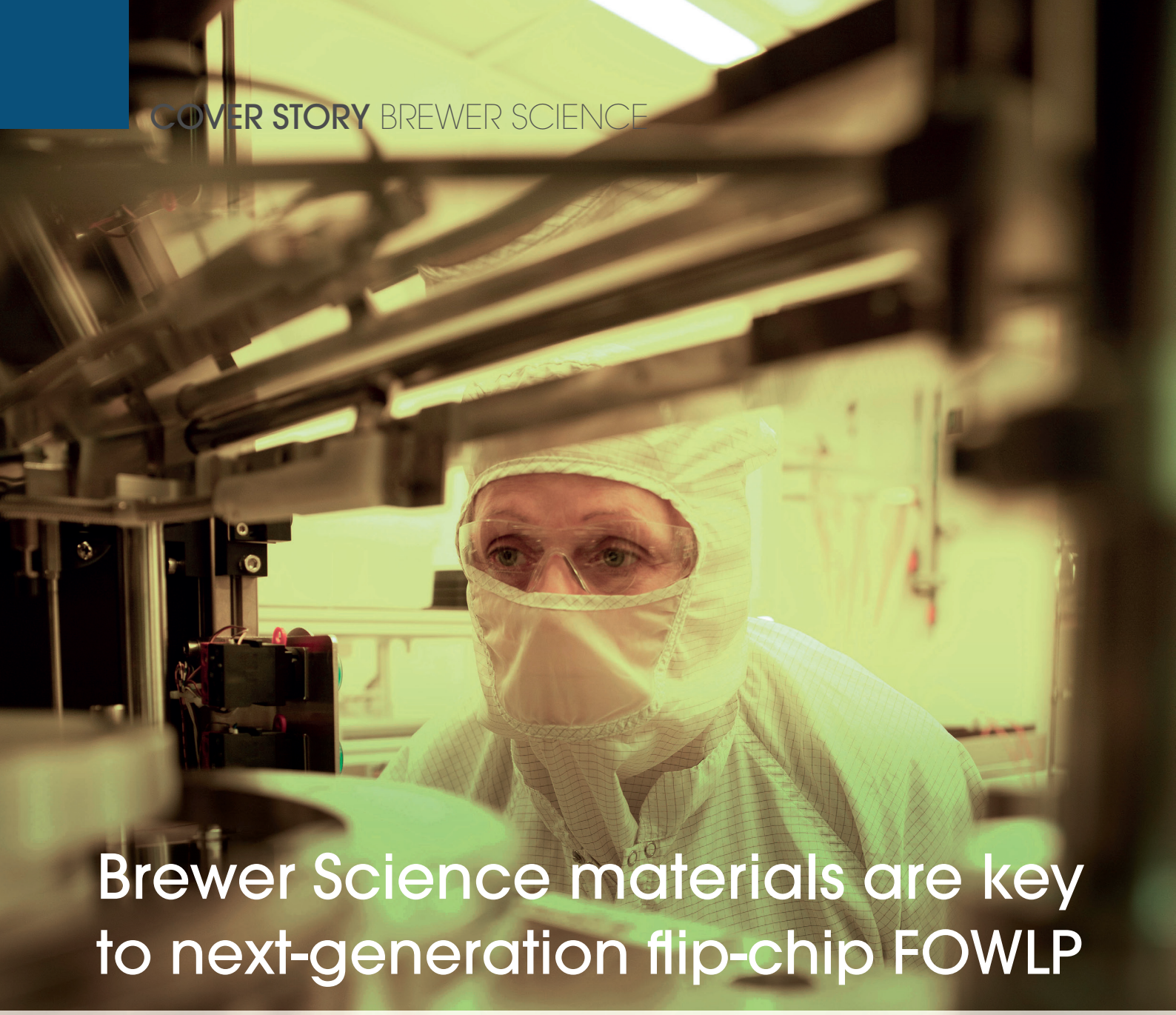

Brewer Science materials are key to next-generation flip-chip FOWLP

Temporary bonding and debonding solutions in many ways enabled the ascendency of 3D structures within silicon semiconductors and are essential to fan-out wafer-level packaging (FOWLP). Stacked dies, utilizing a combination of through-silicon vias (TSVs), microbumps and flip-chip technologies, provide essential connections within die stacks. Advancing FOWLP technologies offer new benefits yet also pose new challenges that are being addressed through innovative materials from Brewer Science.

THE DEVELOPMENT of FOWLP with a greater I/O density, more functionality, smaller form factors and continuing cost reductions is being actively pursued by growing numbers of researchers and manufacturers. But while FOWLP offers many compelling advantages, working with reconstructed wafers and assembling extremely thin dies presents unique challenges including warpage and alignment mismatch that can make further wafer processing a costly challenge. If FOWLP challenges are not addressed at the proper assembly point, yield can plummet and manufacturers can find that the technology they saw as a benefit could instead become a costly miscalculation.

To better appreciate the challenges of FOWLP it is worthwhile to consider some key processing steps, and within that context, to explore the advantages

of next-generation bonding materials that help ensure cost-effectiveness, productivity and higher performance.

With FOWLP, a redistribution layer (RDL) is created to direct I/O connections to the desired die location on the top of the device surface, typically a bump that connects to another die. RDLs can be created either before or after wafer over-molding steps that typically employ an epoxy molding compound (EMC) that has several key roles. The EMC keeps individual components in precise alignment, provides die protection, and enables the integration of dies of different functions and sizes into one wafer.

Assembling and processing dies for FOWLP presents many challenges due to the wide range of temperatures typically utilized, which in turn creates new challenges for temporary bonding materials. One of the main challenges is maintaining device positioning in all three dimensions (X, Y and Z) while at the same time mitigating stress that occurs during the many processing steps required to create a final product.

Temporary bonding materials must deal with high amounts of stress and widely varying process temperatures, all while maintaining wafer geometry, which means reducing bow and warp so it falls within small tolerance ranges.

According to Kimberly Yess, Executive Director within the Brewer Science WLP Materials Division, it was clear that for FOWLP technologies to advance, there was a need for more capable bonding solutions. New approaches were needed to maximize performance, simplify processes and help ensure minimal die shift.

In partnership with imec, a nanotechnology and advanced process research group headquartered in Leuven, Belgium, Brewer Science developed a new generation of temporary bonding solutions that significantly addressed the key objectives. The materials Brewer Science developed in concert with imec provide a range of previously unobtainable benefits, including nearly zero die shift (ZDS), all of which can be achieved using industry-standard equipment.

“The value of new materials in the ZDS process is that it allows for controlled die placement and less adaption of RDL alignment after mold. With correct placement and locking the dies in place, the manufacturing process is more flexible and forgiving to the stresses induced by the EMC. It also allows you to be able to extend the equipment used at the BEOL because of its reduced warp, making it compatible with tools already available,” Yess explained. She noted that when other materials are used to create FOWLP devices, warp and bow can be so pronounced that special BEOL tool sets have been needed to handle wafers that were distorted to the point that malformation could be seen, unaided, by the human eye.

When Brewer Science and imec set out to identify new materials and processing techniques and to test them using standard CMOS-compatible processing equipment, the key challenge was to mitigate the effects of over-molding assembled dies. Researchers are targeting an extremely high interconnect density and believe a 20-μm pitch is now achievable. The technology is highly attractive for mobile device applications since it enables cost-effective memory-to-logic high-density interconnects in a very small form factor. This paves the way for heterogeneous integration that targets high-performance applications.

Flip-chip on FOWLP typically utilizes a mold-first approach in which dies are first assembled on a temporary carrier that is followed by wafer over-molding. In the final step, the RDL is created and connections are made. Expanding on this approach, imec and Brewer Science have shown multi-stacking of chips are efficiently linked using silicon bridges

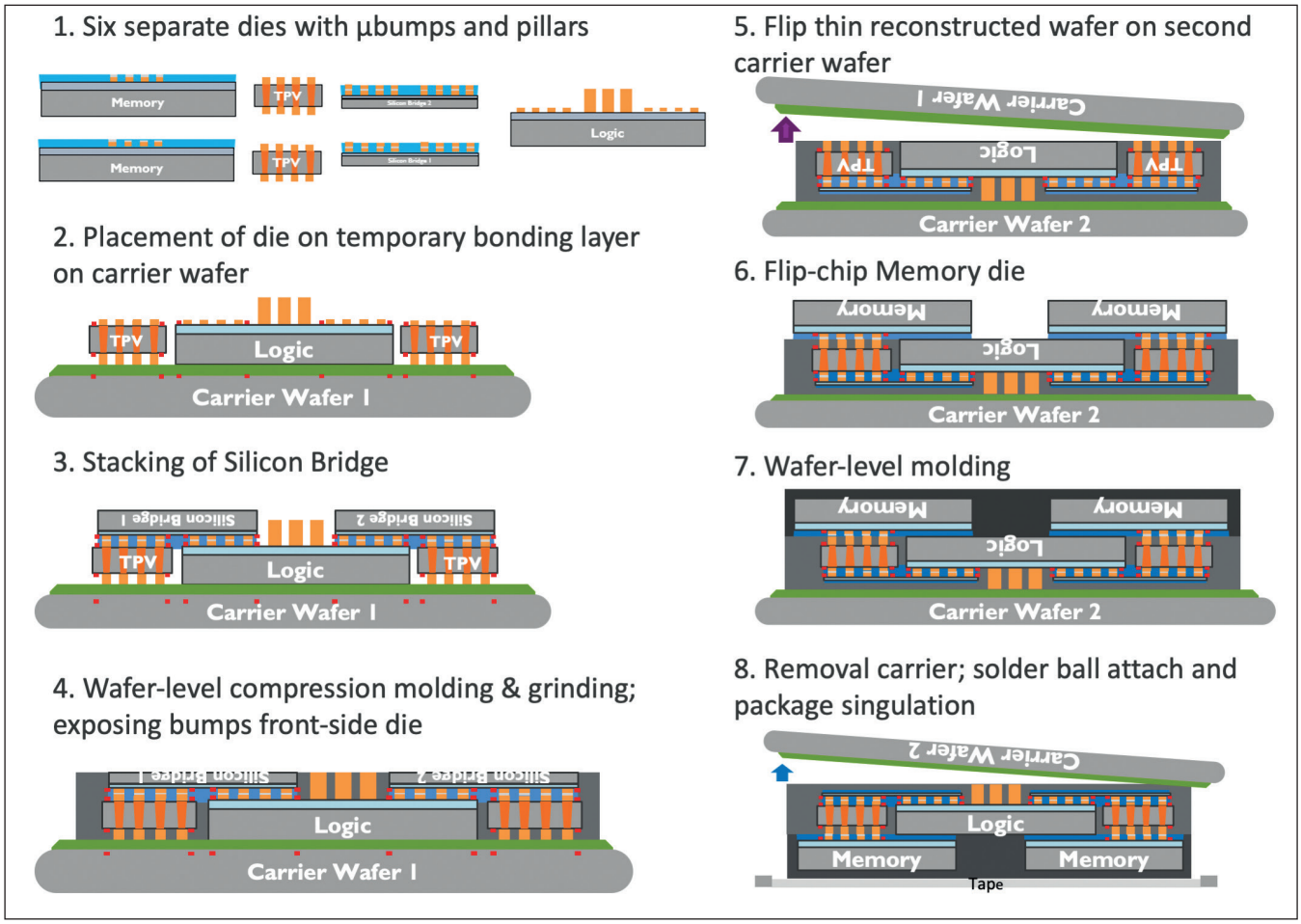

Figure 1: Process Flow Diagram

and through package vias (TPVs) in a two-step molding flow. The feasibility of this approach was first demonstrated using dummy components and is being validated with 'active' dies in subsequent experiments. (See Figure 1: Process Flow Diagram, which illustrates key research goals and findings described in: "Novel Temporary Bonding and Debonding Solutions Enabling an Ultrahigh Interconnect Density FOWLP Structure Assembly with Quasi-Zero Die Shift", Podpod, et al., 68th ECTC, 2018)

The concept that is being developed at imec has multiple steps. The first step is to coat a carrier wafer with a temporary bonding layer (BrewerBOND® C1301 material) and then place the through-package via and logic dies on top. Next, the silicon bridge is attached using thermocompression bonding (TCB). The wafer is subsequently over-molded with an epoxy mold compound.

Following this step the copper pillars are exposed by grinding the mold. After flipping the reconstructed wafer to a second carrier, the first carrier is removed and the memory dies are assembled using a flip-chip technology. A second, wafer-level molding follows; the removal of the second carrier completes this phase of the process flow. The resulting complete package is 300-400 µm thick (excluding solder balls.)

From a materials perspective, it is worth noting that throughout this assembly and processing flow, two temporary carrier substrates are utilized. Success of the entire process is greatly determined by the specific characteristics of the materials coated on the carriers, chiefly: the temporary bonding materials and the release material needed for efficient debonding.

The principal role of the first carrier is to assemble chips with extremely high inter-die alignment: +/- 3 µm, which is needed to allow for the 20-µm bump pitches. To achieve such high accuracy, alignment marks are used in both the carrier and the dies. For these marks to be useful in achieving tight alignment, they have to be visible, which means the first adhesive material must be sufficiently transparent so that precise, automated alignment can occur.

Another key requirement is that the various dies comprising the assembly need to be placed at room temperature, and for a very important reason: limiting or sharply curtailing thermal expansion. Limiting thermal expansion helps enable much more precise die-to-carrier alignment. However, the adhesive also needs to withstand high temperatures during subsequent TCB die-to-wafer bonding steps.

The material must also be able to maintain highly

accurate die placement during the wafer over-molding step that involves heat and force. Finally, to further raise the bar, the adhesive should also allow debonding from the first carrier and be effectively cleaned to reveal the embedded dies for the following process steps.

The second carrier's chief purpose is to enable the removal of the first carrier system without adversely damaging the thinned mold and embedded dies. When it is removed, the front side of the devices can be accessed for testing and further processing by TCB and over-mold.

A major requirement for the second carrier is to enable selective removal of the first carrier without creating die shift, damaging the reconstructed wafer or increasing overall warpage. The adhesive in this case must have very good adhesion to mold and the second carrier while maintaining the ability to debond at the final steps.

The 'enemies' of successful flip-chip FOWLP are die shift, wafer warp and bow. The degree to which dies might move or a wafer could be deformed can also be influenced by the mold material and over-molding techniques that a manufacturer might employ. The initial over-molding takes place after the silicon bridge is placed; the second occurs after the memory dies are attached by flip-chipping them into place. The right choice of temporary bonding and mold materials (and the processes used to apply them) are key to avoiding die shift or wafer distortion after molding.

Imec constructed a number of experiments to evaluate different carrier systems, temporary bonding agents and mold materials. On test blanket wafers, researchers noted that dies maintained their placement accuracy with less than 2 μm shift for both granular and liquid materials. This was true even after exposure to temperatures of 200° C for two hours. Researchers also noted that extremely low warpage of less than 200 μm was achieved across the entire 300-mm wafer.

These experiments demonstrated warpage values far below those reported in literature. For example, warp is typically on the order of millimeters to centimeters - you can measure it with a ruler. However, with advanced bonding materials and advanced mold materials, warp is reported on the micron scale.

Just as temporary bonding materials and over-molding materials are essential to successful flip-chip FOWLP processing, so is efficient debonding for carrier systems. In the case of carrier one, it was found that mechanical debonding was most successful and did not impact the second bonding process. A laser-assisted debonding process was found to be most effective for successfully debonding the second carrier since it aided selective debonding.

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Conclusion

Imec's development of an innovative new approach to flip-chip FOWLP technology shows a path forward to reducing warp and bow in high density interconnect packaging that also demonstrates a way to help ensure dramatically reduced die shift. The Brewer Science temporary bonding adhesive, Brewer Bond® C1301 material, plays an essential role as a key enabler of these advances. The fact that the process, paired with essential new materials science, has produced very low warpage is key to processing over-molded substrates in standard manufacturing equipment.

The need for specialized process tools designed to handle reconstructed wafers that exhibit significant warpage can be eliminated. The fact the temporary bonding agent is designed for application at room temperature while still being able to sustain stability at temperatures up to 200° C for two hours is a significant milestone. Fine pitch RDLs in combination with a chip-first will pave the way for a wide range of applications, especially those in which the end goal is high density I/Os.

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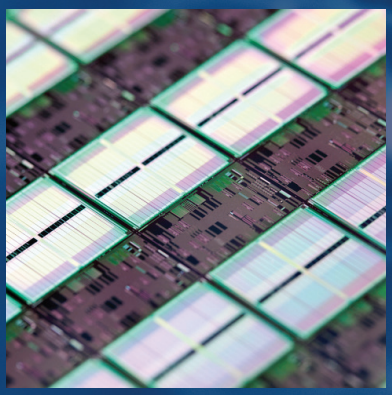

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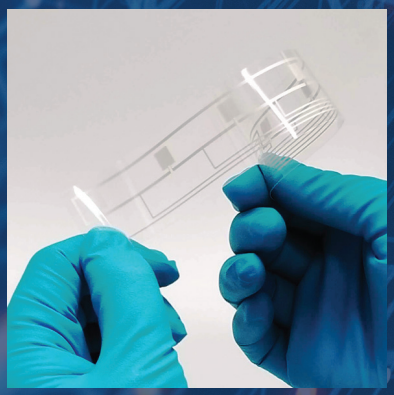

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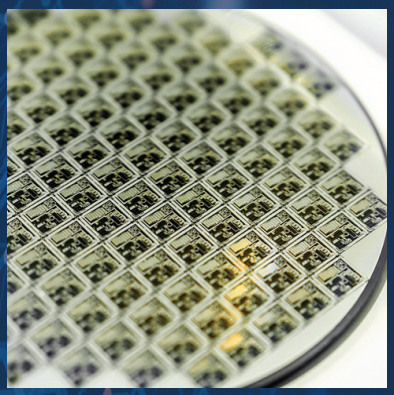

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