Advancements, Versatility, and Flexibility of Dual-Layer Material System for Advanced Packaging Applications

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Abstract

Integrated circuits (IC) have seen a major shift in development within the past 10-20 years with traditional lithography methods showing a drastic increase in development time for more advanced nodes, as well as an exponential increase in cost to achieve the same performance gains as before. The increase in cost and the decline in development in lithography have resulted in looking at advanced packaging technologies to achieve the same performance gains by changing the way IC design is approached. The look towards advanced packaging technologies for the future in terms of increasing performance for a substantially lower cost has resulted in considering the IC as a system of components working intertwined with each other rather than as individual components. This shift in mindset has resulted in technologies such as system in package (SiP), package on package (PoP), and fan-out wafer-level packaging (FOWLP). One advanced packaging technology that plays a critical role enabling these aforementioned technologies is temporary bond and debond (TB/DB). TB/DB's crucial role in advanced packaging is due to the enablement of backside processing such as wafer thinning, bumping of the wafer, die stacking, and chemical vapor deposition/physical vapor deposition (CVD/PVD)–type processes by the use of a support carrier wafer. The support carrier wafer also allows for the use of highly warp-prone materials such as epoxy mold compound (EMC), which are critical in FOWLP applications, by reducing the overall warpage of the entire wafer stack. To utilize the support carrier wafer, a robust material solution is required to allow for the wafers to be bonded together and subsequently released after backside processing by one of the primary separation methods of thermal slide, mechanical, or laser debond.

Brewer Science has designed and developed a dual-layer temporary bonding system. This system consists of two materials, a thermoplastic layer that is typically coated on the device, and a thermoset layer which is typically coated on the carrier. The materials developed for the dual-layer system demonstrate very good performance in very high temperature applications, EMC wafer handling, and device thinning to sub-20 µm. In this paper, we will summarize their capabilities and introduce how adhesion between the two temporary layers can be adjusted by material design. We will also cover a new feature of the thermoset layer that can be patterned to allow for the use of a patterned bonding material for TB/DB-type applications.

Key words

Temporary Wafer Bonding, Dual-Layer System, Photopatterning, Thermoplastic Materials, and Thermoset Materials

I. Introduction

Expectations for wafer-level packaging (WLP) technologies continue to escalate as the industry seeks solutions to higher-performance and lower-cost requirements for advanced semiconductor devices. Sacrificial materials for temporary bond and debond (TB/DB) have enabled advanced processing approaches including fan-out wafer-level packaging (FOWLP), system in package (SiP), and package on package (PoP). During development of new device generations with increased complexity utilizing these technologies, previous TB/DB materials often have performance characteristics that are suitable for only a narrow range of specific applications. However, Brewer Science's Dual-Layer System (DLS) was developed to achieve versatile performance capabilities while processing numerous semiconductor device types.

For this two-layer system, the thermoset material, spin-coated on a transparent carrier wafer, can be cured after bond with different techniques – thermal energy typically delivered by proximity bake plate, broadband ultraviolet (UV) light exposure through a glass carrier wafer, or a combination of both. Curing method tunability allows for processing of thermally sensitive device structures and reduction of overall warp for bonded pairs with high coefficient of thermal expansion (CTE) mismatch by initiating material cure with cooler wafer temperatures [1].

Materials with different thickness ranges are commercially available within the DLS portfolio. Versions designed for thin bond lines can minimize total thickness variation (TTV) for applications with tight uniformity specifications. Thick thermoset materials minimize bond voids and stress-induced edge delamination when processing structures with deep features, high warp, or CTE mismatch. Selectable thermoplastic material viscosities enable optimization of conformal material coverage for confined cavity openings and high-aspect-ratio device topographies [1,2].

Following bond and cure of DLS-coated samples and subsequent backside processing of device wafers, controlled separation at the interface between thermoset and thermoplastic layers can be accomplished using two different approaches – edge-initiated mechanical debond or raster-scanned UV laser exposure. All DLS material combinations support either debond method, so generational process development adjustments that require a different separation technique can use the same TB/DB layers [3,4].

As semiconductor device designs continually become more complex, expanded capability of TB/DB material performance is demanded from the industry. This includes enhanced bond-line robustness during extreme back-end process operations and the possibility of UV laser debond to separate this high-adhesion interface. More fragile localized device structures, such as micro electro-mechanical systems (MEMS), require improved protection from high-adhesion damage and surface contamination by defining specific contact areas of bond material [5]. Also, for double-bonded wafer stacks, more versatility is desired in debond options by controlling adhesion differences between the two bond interfaces on either side of device wafers [6].

In this paper, we demonstrate how these capability needs can be addressed with modification to DLS processing or materials, further broadening their versatility to semiconductor processing. Significant adjustment to adhesion between DLS thermoplastic and thermoset materials is achieved by material design. Also, the UV sensitivity of the thermoset material is extended to a new functionality that enables photo patterning of TB/DB material.

II. Material characterization

The DLS utilizes a thermoset bonding layer, Material A, with a variety of thermoplastic layers, Materials B and C, to allow for processing at higher temperatures. Material A, the bonding layer, is designed to cure at temperatures at or below 220°C to allow for the material to be set in place to stop material flow at higher temperatures and to prevent bond-line voiding that is common with standard thermoplastic bonding layers at elevated temperatures. With Material A having the ability to cure at higher temperatures, it also needs enough material flow at lower temperatures to enable bonding, which requires a low enough T_g (glass transition temperature) to have an acceptable melt viscosity profile. The contrast between the onset of cure and the low enough bonding temperature can be seen in the melt viscosity curve in Figure 1. Materials B and C are each designed to be a tough rigid layer that has a high T_g and high Young's modulus to allow for the material to exhibit no material flow even at high temperature but remain solvent-cleanable due to the nature of the uncrosslinked films. The high T_g and high Young's modulus allow for these materials to be used at elevated temperatures where they can be conformally coated on devices and remain in place on topography as well as act as a controlled separation interface with Material A and the device by either method of mechanical or laser debond. The T_g and the T_d (thermal decomposition temperature) at 1% weight loss under N_2 of the materials can be seen in Table 1. The Young's modulus of Materials A, B, and C can be seen in Table 2.

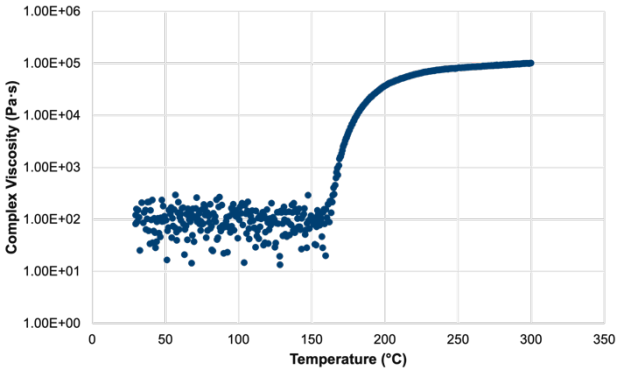

Figure 1. Melt viscosity profile of Material A

Table 1. Thermal Properties of Materials A, B, and C

Material	Glass Transition Temperature (°C)	1% Weight Loss Under N_2 Thermal Decomposition Temperature (°C)
A	<-50 (Pre-Cure)	420
B	328	465
C	225	375

Table 2. Young's Modulus of Materials A, B, and C

	Material A	Material B	Material C
Young's Modulus (MPa)	3.3	2900	2553

Material A has a much lower Young's modulus compared to Materials B and C which is beneficial in reducing the over stress and subsequent stack warpage induced by the bonding layer as it will be the thickest material in the TB/DB bonding stack.

Along with Young's modulus, optical properties are important for Materials B and C due to the need to support laser debond at conventional laser wavelengths. Table 3 shows the n, index of refraction, and k, extinction coefficient, values for the two materials.

Table 3. n & k of Materials B and C

Wavelength (nm)		308		355	
		n	k	n	k
Material	B	1.90	0.09	1.77	0.03
	C	1.86	0.08	1.76	0.01

III. Experiment

Overview

A series of experiments were set up to evaluate the DLS as a potential solution for a variety of different TB/DB applications.

Process Conditions

The DLS uses a variety of spin conditions for the different materials. Table 4 shows the spin and bake conditions as well as typical thicknesses used to process the DLS materials.

Table 4. Process Conditions of Materials A, B, and C

Material	Spin Conditions	Bake Conditions	Thickness
A	650 rpm 500 rpm/s 90 s	60°C, 1 min 120°C, 2 min Post-bond Cure 180°C, 5 min 220°C, 5 min	50 µm
B	1200 rpm 1250 rpm/s 45 s	220°C, 2 min	2 µm
C	700 rpm 1000 rpm/s 30 s	60°C, 1 min 220°C, 4 min	2 µm

In Table 4, the standard process conditions including the standard thermal cure are shown for Material A. In place of the thermal cure, an optional UV exposure of 60-150 mJ/cm^2 can be performed to lower the temperature requirement of the curing to 120°C for 5 minutes.

There is flexibility in the process conditions shown in Table 4 to obtain a wide variety of thicknesses by either tuning spin conditions or using different formulations targeted at different coating thickness. Bonding for the DLS materials was done for 200-mm wafers utilizing an EVG 510 bonder and for 300-mm wafers using a CEE® Apogee™ bonder, and typical bond conditions for Material A are shown in Table 5.

Table 5. Bond conditions for Material A

Material	Temperature (°C)	Force (N)	Time (min)
A	25	0	3

Debond Equipment

Laser release of wafer pairs was done by using a 308-nm laser wavelength (Süss ELD12 laser debonder) and a 355-nm laser wavelength (Kingyoup LD-Semi Automatic 200/300). Mechanical release for wafer pairs were done by using a Süss DB12T mechanical debonder.

Metrology

Material thickness and bow and warp measurements were measured using an FRT MicroProf® 300 optical metrology tool. CSAM (Confocal Scanning Acoustic Microscope) imagery was obtained using a Sonix EHCO VS™ ultrasonic tool.

Adhesion Testing

The adhesion of the DLS materials and modifications made to Material A was measured by utilizing a razor blade

insertion test method; the Maszara model was used to calculate the bond energy between the two materials [7,8]. An example diagram for the setup for the bond energy test method is shown in Figure 2.

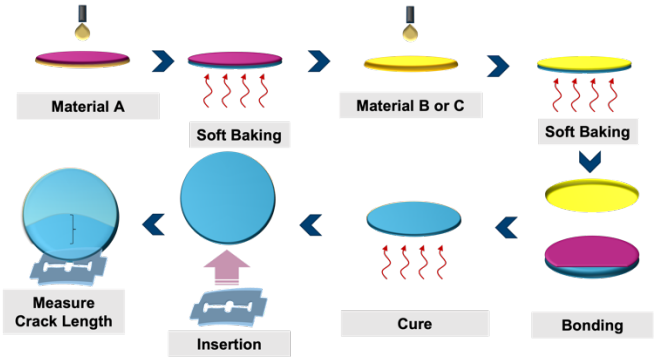

Figure 2. Razor blade insertion test method

Along with the adhesion at the interface between Materials A and B/C, the adhesion of Materials B and C to the substrates on which they are coated was quantified by the stud pull adhesion test method. An example tester and the setup for the stud pull adhesion testing can be seen in Figures 3 & 4, respectively.

Positest adhesion tester, conforming to international standards including ASTM D4541/D7234/D7522, ISO 4624/16276-1, AS/NZS 1580.408.5 and others.

Figure 3. Example tester for stud pull adhesion testing

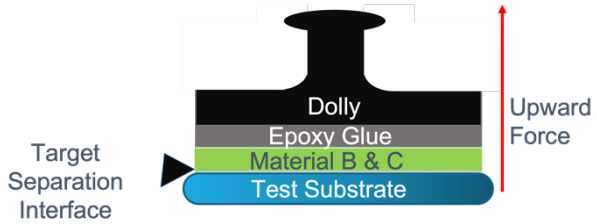

Figure 4. Testing setup for stud pull adhesion testing

Photo-Patterning

Photo-patterning of Material A was done utilizing a Süss MJB4 Mask Aligner with a broadband lamp source and hard contact mask. The pattern process of Material A had an exposure dosage of 68 mJ/cm^2 followed by post-exposure bake at 120°C for 5 minutes. The uncured material was removed utilizing a 4-minute solvent soak and 30-second rinse of mesitylene followed by a 15 second rinse in isopropyl alcohol (IPA).

Cleaning

Cleaning of the thermoplastic layers for the DLS is very important so that the device can be used after all the processing is finished during the TB/DB process. There are a variety of ways to clean the materials, but a solvent-based spin clean process is typically one of the preferred methods of cleaning. The thermoplastic materials can be cleaned utilizing a Süss MicroTec SD12 or AR300TF wet processing system with a tape protection ring to protect the dicing tape from the solvent. A puddle-spin clean process can be seen in Table 6 with a total clean time of 200 seconds and 150 ml of solvent consumed, and a high-pressure spray-spin clean process can be seen in Table 7 with a total clean time of 100 seconds and 100 ml of solvent consumed. Both processes utilize 1,3-dioxolane as the cleaning solvent.

Table 6. Puddle Spin Cleaning Process

Step	Spin Speed (rpm)	Operation
1	0	Set Tape Protection Ring
2	50	Dispense
3	0	Soak
4	500	Short Spin
5	0	Dispense
6	0	Soak
7	1500	Spin Dry
8	0	Release Tape Protection Ring

Table 7. Pressure Spray Cleaning Process

Step	Spin Speed (rpm)	Operation
1	0	Set Tape Protection Ring
2	500	Pressure Spray, Start
3	500	Pressure Spray, Move
4	500	Pressure Spray, End
5	1500	Spin Dry
6	0	Release Tape Protection Ring

IV. Results and Discussion

TB/DB utilizes a carrier wafer to support a device wafer that will undergo back side processes; some of these backside processes include backside grinding, PECVD, and photolithography. Utilizing the DLS, the general process flow is shown in Figure 5.

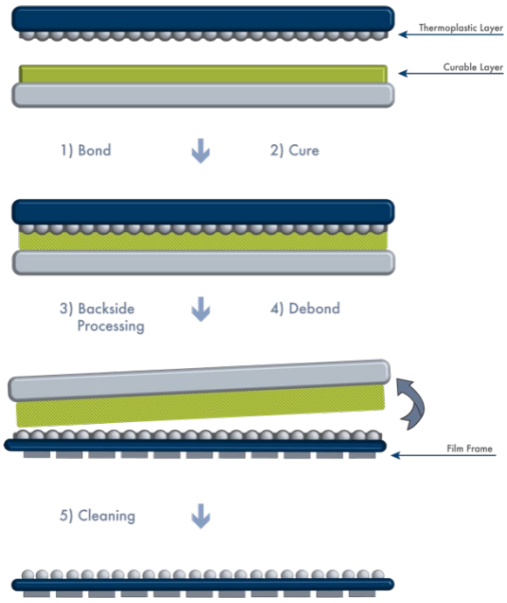

Figure 5. TB/DB Process Flow for DLS

The aforementioned processes go hand in hand with a variety of applications within TB/DB that have their own unique challenges for the materials that will support the processes. Some of the challenges include: high temperature processing of thinned wafers, high topography device wafers, epoxy mold compound (EMC) wafers, high-stress processes, or the need to encapsulate a device to protect it from material contamination.

High-Temperature Wafer Processing

One major challenge for TB/DB materials is the processing of thinned wafers at high temperatures for long times. This process can be difficult for a variety of reasons. The first reason is that typical thermoplastic bonding materials exhibit a significant drop in their melt viscosity profile which results in too much material flow at the elevated temperatures, causing void formation from the material flowing out of the bond line. The second issue involves induced stresses due to all the different materials in the wafer stack and processes that might require high temperatures (PECVD, high temperature annealing, etc.) which result in damage to the thinned wafer if not properly managed. There can be many approaches to tackling these problems. For the first problem of material flow, utilizing a thermoset layer with high-T_g thermoplastic can be beneficial as it minimizes the interactions that material flow can cause in the bonded wafer stack. The second problem, stress, is a little more complicated and can have numerous approaches. For example, the thickness of the bonding layer can be minimized to reduce the impact of stresses the bonding layer induces on the system. Another approach, adopted by DLS, is to use a softer thermoset layer that induces very little stress onto the wafer structure as well as helps absorb other stress in the system. To test the DLS materials at these elevated temperatures, 300-mm wafer pairs were prepared by bonding a Si carrier wafer coated with 30 µm of Material A and a blank Si wafer (acting as the device wafer) coated with 2 µm of Material B. After bonding, the wafer pair was inspected for voiding in the bond line by CSAM, shown in Figure 6A. The bonded wafer stack then underwent Si device wafer thinning down to 30 µm, was heat treated under vacuum at 300°C for 220 minutes, and inspected again by CSAM, as shown in Figure 6B.

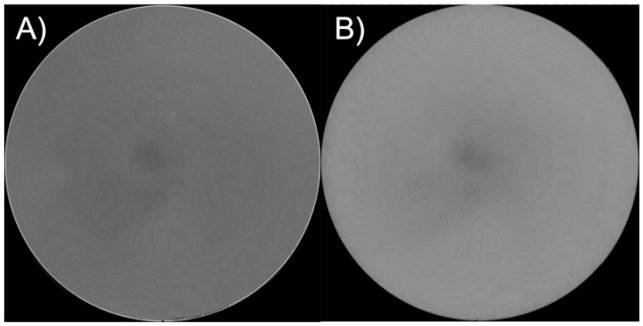

Figure 6. A) CSAM image of Material A/B wafer pair after bond and cure. B) CSAM image of Material A/B thinned wafer pair after high temperature treatment

On inspection of the CSAM images of the wafer pairs, there is no visible voiding, which would typically appear as black or white spots. No detectable voiding is observed in either the bond and cure sample or vacuum-heat-treatment bonded pair.

Conformal Coating

Due to the unique nature of the DLS materials, the material set must be able to coat over topography efficiently. Coating the thick curable layer on the carrier results in having to use the thin thermoplastic layer on the device. The thermoplastic layer is typically thinner than 5 µm and cannot fill in the spaces on a wide variety of topographies, since a very thick layer could induce elevated stress on the device. If the release layer is not able to conformally coat the device, then the curable layer will be in direct contact with localized device regions resulting in cleaning difficulties as well as potential damage in larger features such as solder bumps and pillars due to lack of support in higher temperature processes. Examples of this damage can be seen by SEM (scanning electron microscope) imagery in Figure 7A where unoptimized conformal coating of Materials B and C was applied to 80-µm solder bumps; examples of undamaged 80-µm solder bumps from optimized conformal coating conditions are shown in Figure 7B.

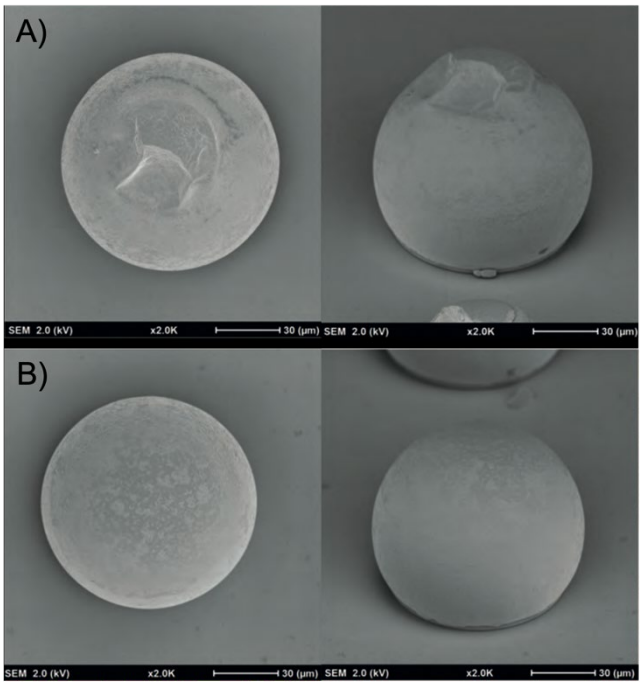

Figure 7. A) Example damages of solder bumps with unoptimized conformal coating. B) Successful protection of solder bumps

The topography on which the thermoplastic layer must cover varies based on the device, and each type of topography has its own unique challenges to obtain efficient conformal coating. For the solder bumps shown in Figure 7, topographical details such as the radius of curvature of the bump can heavily impact how well a material conformally coats, so Materials B and C must be able to coat over drastically different topographies. In Figure 8, one such topography variation is shown where a modified solution of Material B was applied to a 60-µm copper pillar with a rounded top; continuous thermoplastic material coverage is demonstrated on pillar sides and top.

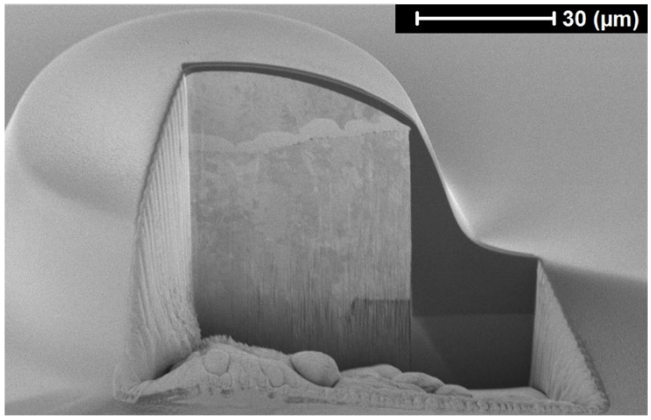

Figure 8. Conformal coating of Material B over 60-µm copper pillar

EMC Processing

EMC wafers are commonly encountered in advanced packaging with FOWLP being a popular use case. These types of wafers are typically made by a molding process that is performed on a carrier wafer with or without dies utilizing an epoxy resin that contains a large portion of silica filler to enable lower CTE. The reconstituted wafer that comes from the molding process presents several difficult problems, such as excessive outgassing at higher temperatures, weak adhesion to a wide variety of materials, and extreme warp when exposed to elevated temperatures due to the high stresses within the wafers. Due to the high stresses, lower-T_g thermoplastic bonding layers can have issues adhering the EMC wafer to a carrier wafer at elevated temperatures; low-T_g material can flow too much and essentially reflow away from the surface of either the EMC or the carrier wafer as stress builds up in the wafer pair. To address the problem of material flow at elevated temperatures, a curable layer is desirable, but utilization of curable layers also has its own unique challenges.

EMC wafers introduce a handful of challenges for curable layers due to the requirement of lower-temperature processing. The need to utilize low-temperature processing can make material choice for thermoset layers tricky: this causes the curable layer to be designed around a curing mechanism that allows for reduced-temperature processing to minimize warp. This curable layer also needs to be processed without further inducing stress on the EMC wafer stack. To reduce the amount of stress that is imposed on the stack by the curable layer, a softer curable material that has the option to be either UV- or thermally cured can be highly beneficial in this case. Our previous work has demonstrated that by using a softer curable layer with a high-melt-viscosity thermoplastic, the EMC wafer can be handled well. For example, a rigid curable material with a thin glass carrier exhibits severe wafer bow after a 250°C heat treatment for one hour. Figure 9 shows the pictures of wafer pairs after heat treatment without and with the DLS materials. [4]

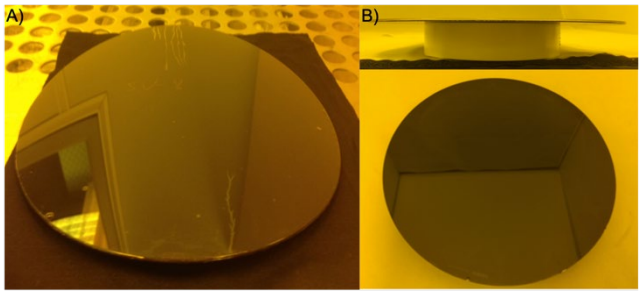

Figure 9. A) 250°C 1-hour-heat-treated EMC wafer pair with rigid curable material, B) 250°C 1-hour-heat-treated EMC wafer pair with DLS materials.

The EMC wafer bonded with DLS materials can be separated by mechanical or laser debonding methods. Figure 10 shows the glass carrier wafer and EMC wafer after laser separation at 308-nm wavelength.

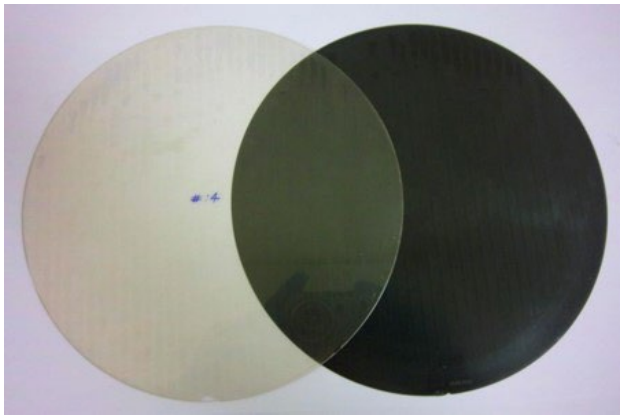

Figure 10. EMC and carrier wafer post-308-nm laser debond

Tunable Adhesion

The DLS was originally developed as a material system capable of mechanical debond as well as laser debond. The need to mechanically debond versus the need to laser debond can cause some complicated issues. One of the issues can be attributed to adhesion of either the materials between each other or the materials with the substrates they are coated on.

Mechanical debond is a method that requires the adhesion between the two material layers to be not only low enough that materials can separate at their interfaces after processing, but also high enough that materials remain in contact with each other through all the processing. Laser debond, on the other hand, does not require a maximum post-coat material adhesion for separation as laser debond ablates material at the interface allowing for as high of adhesion as possible. Due to the difference between laser and mechanical debond, the laser approach typically handles high-stress applications better than mechanical debond because of the fundamental upper limit on adhesion with mechanical debonding.

With laser debond not having an upper limit on adhesion, Material A was investigated for its ability to have tunable adhesion by making minor modifications to the system that does not affect the fundamental properties of how Material A interacts with Materials B and C. Three modifications to increase adhesion were made to Material A and then the modified versions of Material A were bonded to the thermoplastic layers. The adhesion between the curable and thermoplastic material layers was measured via the razor blade insertion method shown in Figure 2, and the results are shown in Table 8.

Table 8. Adhesion modification results of Material A to Material B

	Crack Length (cm)	Bond Energy (J/m^2)
Material A	3.01	0.16
Material A-1	2.76	0.22
Material A-2	2.94	0.18
Material A-3	2.34	0.44

The results in Table 8 show a wide tuning range of the system by having only minor adhesion increases (Materials A-1 and A-2) or a major adhesion increase (Material A-3) of more than 2x of original adhesion between the material layers.

Adhesion tunability is important for not only the thermoset layer to the thermoplastic layer but also the thermoplastic layer to common substrate types. The two thermoplastic materials, Materials B and C, were measured for adhesion to a variety of substrates using the stud pull adhesion method described in Figures 3 and 4. The results can be seen in Table 9.

Table 9. Adhesion of Materials B & C to different substrates

Substrate	**Material B**	**Material C**
Si	31 psi	>33 psi
SiO_x	27 psi	42 psi

In Table 9 it is shown that Material C can obtain higher adhesion to both Si and SiO_x while just slightly lowering thermal stability (T_d) of the thermoplastic layer.

Photopatterning

The dual-layer material system has already been shown to have a large amount of flexibility in applications. The thermoset layer in the DLS offers even further flexibility in that it can have the ability to photopattern and allows for reduction or elimination of thermal cure by UV exposure. The photopatterning of Material A could be of interest in applications that may not need temporary bond solution that provides full support via the entire area of a carrier wafer, but instead selective bonding of dies or areas of wafers to give support in critical areas.

In order to test the photopatterning of Material A, the material was spin coated on a 4” wafer at a thickness of 30 µm and was baked free of any solvent. The Material-A-coated-wafer was then patterned and developed in a mask aligner utilizing the mask shown in Figure 11 and the photo-patterning conditions previously mentioned in this paper.

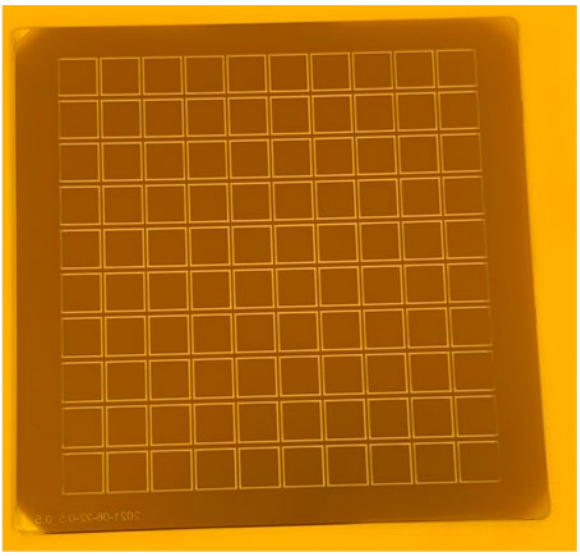

Figure 11. Photo-mask used for patterning test

After patterning and development, the wafer was both visually inspected and inspected utilizing a 3D laser scanning microscope (Keyence VK-X1000). The patterns that were formed showed the bulk areas of the squares were cleaned out, and the width of the features were 550 µm. The wafer image as well as the microscope image can be seen in Figure 12 A & B.

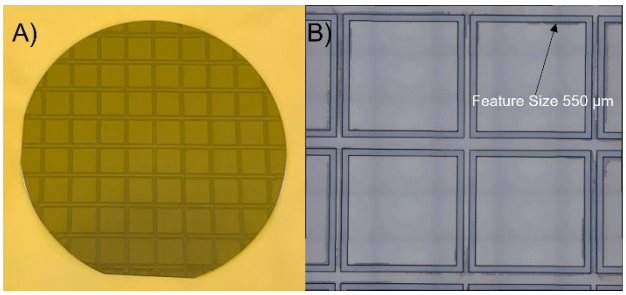

Figure 12. A) 4" Wafer with Material A after patterning and development. B) Microscope image of patterns in Material A

After the pattern testing was performed, a separate test for bonding of the cured material was performed. For this testing, Material A was coated on an 8" Si wafer, manually processed through EBR (edge bead removal), subjected to blanket wafer exposure at the same dosage as the patterned wafer, and then bonded utilizing the conditions shown in Table 10.

Table 10. Bond conditions for cured Material A

Bond Force	Temperature	Time
1500 N	60°C	3 mins

The wafer pair where Material A was blanket-exposed (cured) first and then bonded can be seen in Figure 13. It can be seen that the majority of the wafer surface is void-free with some minor voiding in the manual EBR area of the wafer which can be attributed to the way the EBR was performed.

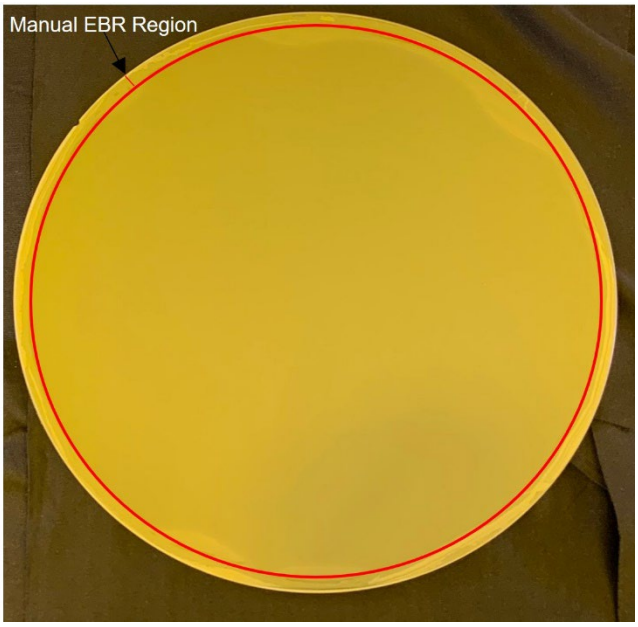

Figure 13. Material A after curing – bonded 8" wafer pair

V. Conclusion

Brewer Science's Dual-Layer System is unique in its design to enable the materials to have large amount of versatility in application choice and properties. The DLS materials allow for the use of a soft curable layer in EMC wafer processing to reduce warpage induced by the thicker bonding layer as well as has the versatility to be either laser or mechanically debonded. The thermoplastic layer offers the ability to be used on a variety of topographies to enable protection of topography as well as a clean separation interface from the curable layer. The curable layer has the ability to have tunable adhesion to the thermoplastic layers, and the thermoplastic layers can have tuned adhesion to a variety of substrates. Finally, the curable layer has the ability to be photopatterned for a variety of applications where selective area bonding could be desired to provide support in critical areas for dies or wafers.

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